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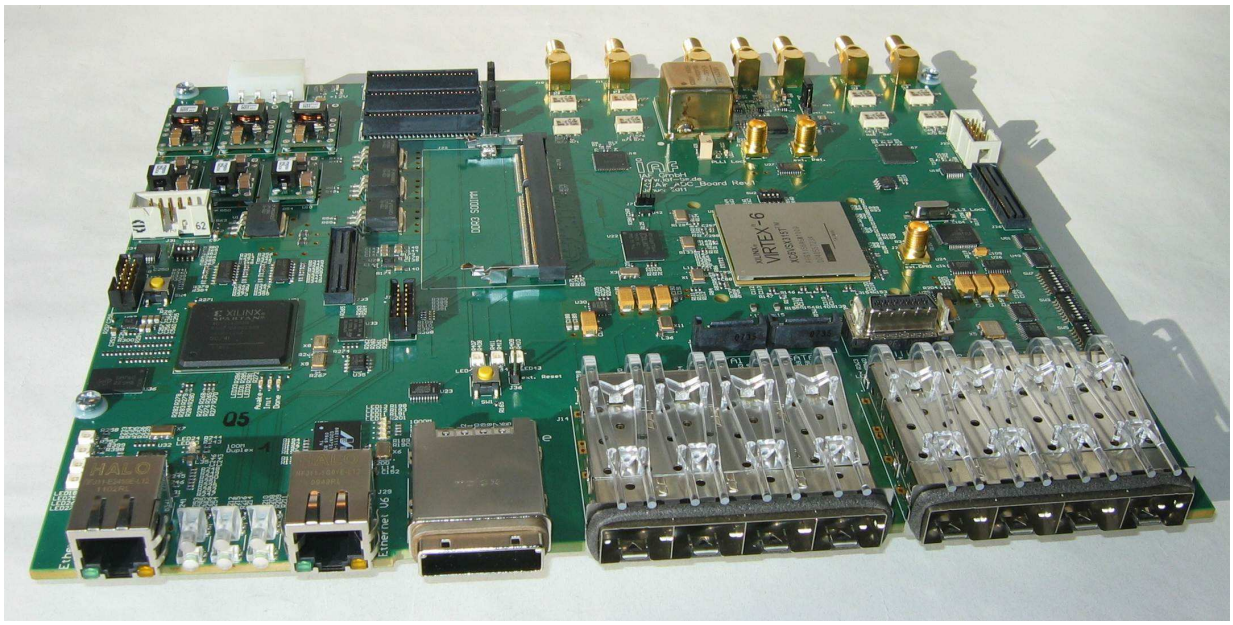
Virtex6 ADC Board (Rev. 1.0)

(Data Sheet Rev. 1. April 2011)

1. Overview



The Virtex6 ADC Board is designed for four channel A/D conversion and digital post-processing. It supports several serial high speed interfaces like CPRI, PCIe, SATA, SRIO and Ethernet.

In a typical application the Xilinx Virtex-6-SXT FPGA is used for digital down-conversion and filtering of the received ADC data streams and for controlling of the connected analog RF circuits. Two double 14-bit ADC converters (ADS62P49) are included on board for converting analog signals to digital data streams. Additionally the board includes a Spartan 3AN FPGA for hardware programming and monitoring purposes via own Ethernet interface.

Applications:

- Digital down-conversion and baseband processing
- Multiplexing and conversion between serial interfaces (CPRI / OBSAI / SRIO / PCIe)

- High speed data capturing with up to 4 GByte DDR3 memory on board

The board includes following digital data interfaces:

- 1 x PCI Express Interface with 4 Lanes
- 2 x SATA Interface
- 1 x SRIO Interface with 4 Lanes
- 3 x Parallel Interfaces
- 8 x SFP Interface
- 1 x 10/100/1000 Ethernet Interface (Virtex6)
- 1 x 10/100 Ethernet Interface for Hardware Programming and Monitoring (Spartan3AN)

The complete clock generation and power supply is integrated on board (see Figure 1).

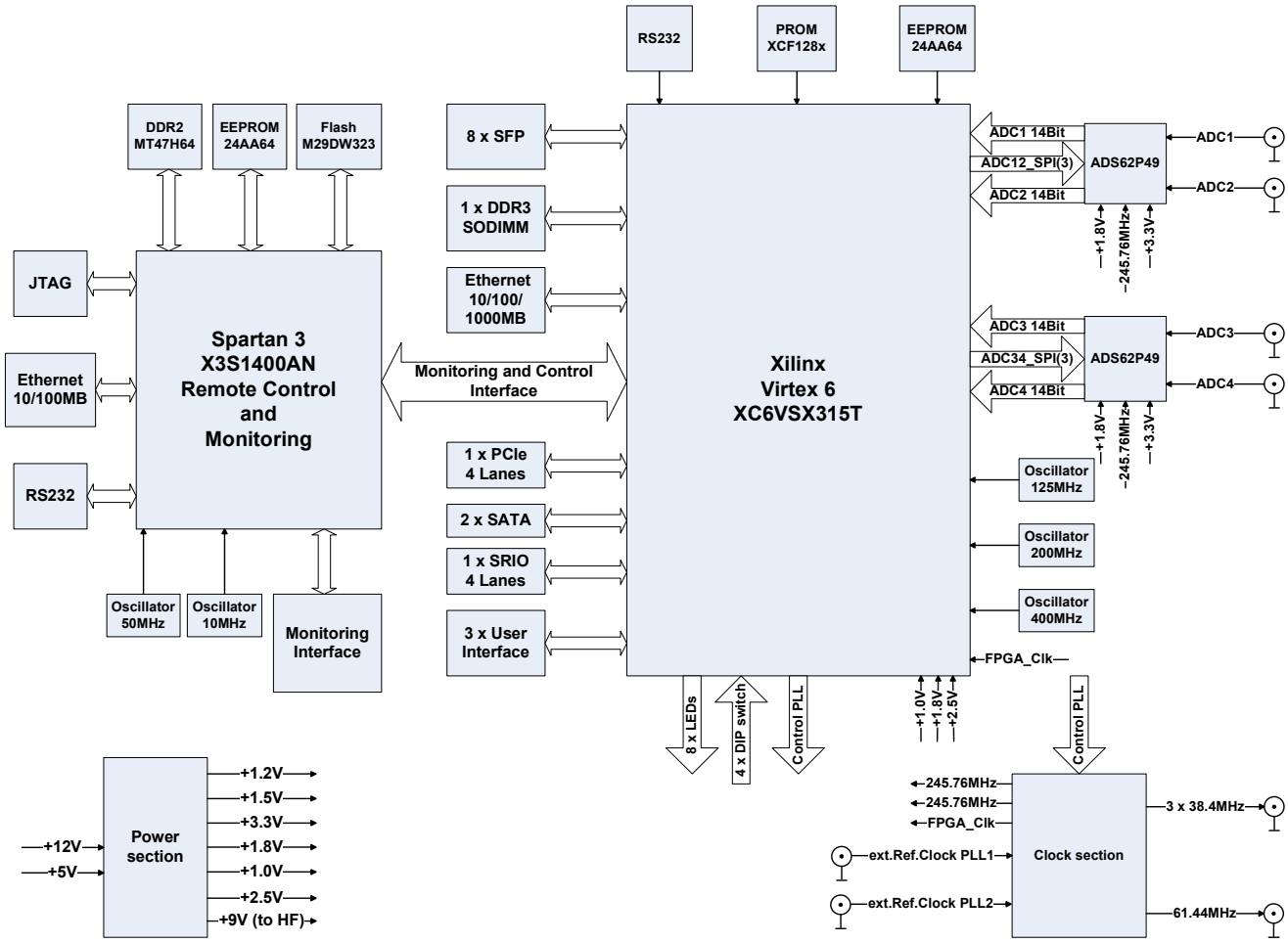


Figure 1: Block Diagram

The Virtex6 FPGA can either be configured directly via Ethernet, JTAG-Interface or via an integrated flash ROM configuration memory.

2. Power Section.

The Virtex6 ADC Board includes the complete power generation on board and needs only +5V voltage input. The analog domain supply voltage for A/D conversion is generated separately with linear voltage regulators (see Figure 2). The +12V input is used for generating the power for external hardware like HF modules etc.

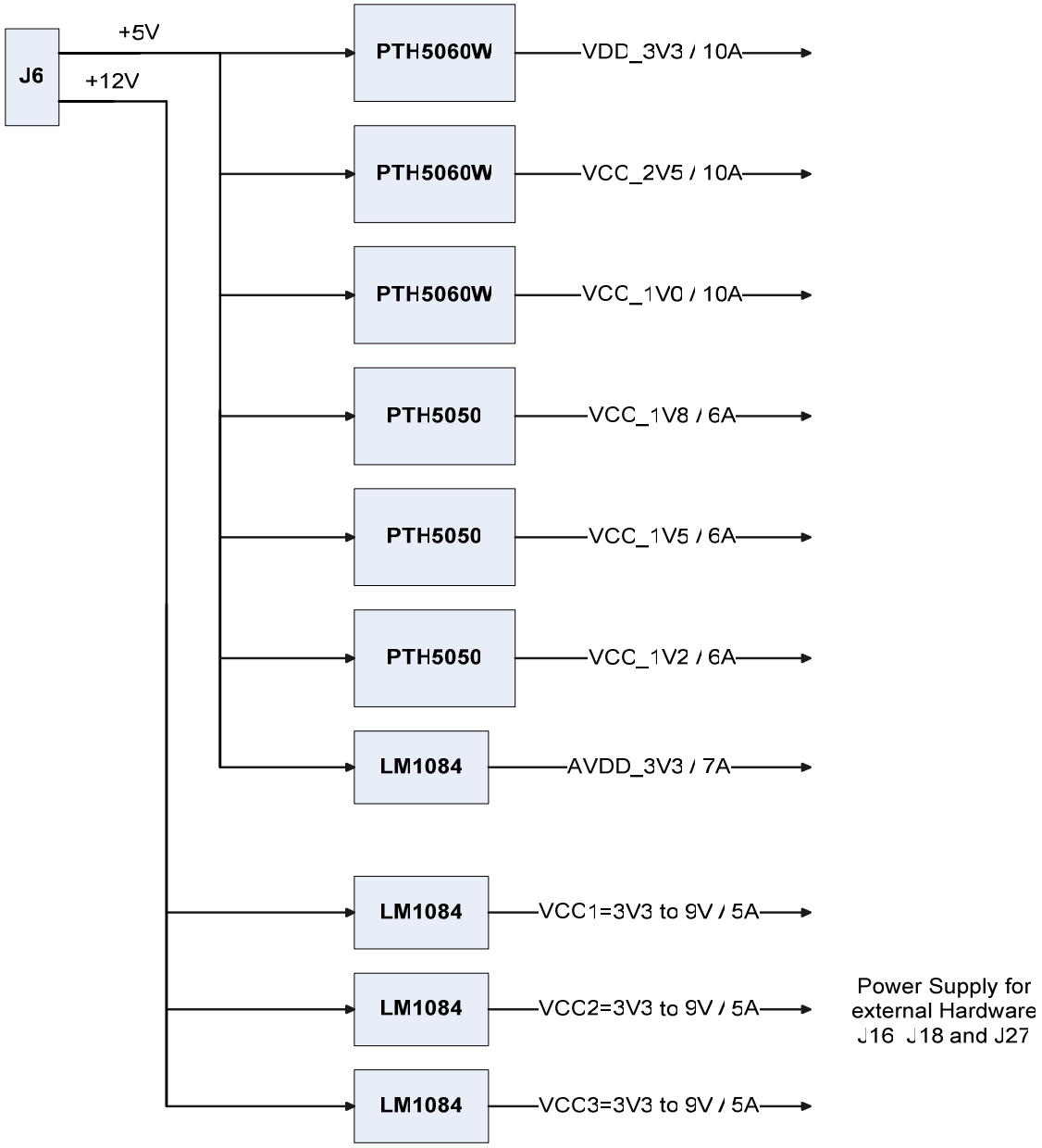


Figure 2: Power Section

3. Clock generation and distribution.

The board includes the complete clock generation and distribution. The internal VCO of PLL1 can generate clocks in range from 2270MHz to 2650MHz. This clock will be divided and distributed to different outputs and is used to generate clocks for AD converters. The AD9520-1 can work with input reference clock from 10 to 250MHz. The reference clock can be provided from oven oscillator (38.4MHz) or from external connector J4. The second PLL is used to generate clocks for MGT's of Virtex6. The reference can be provided on three ways to PLL2:

- oscillator X10 (30.72MHz)
- external connector J20
- Virtex6 (U15). This can be used for CPRI clock recovery

Both chips are programmable from Virtex6 (see Table 1).

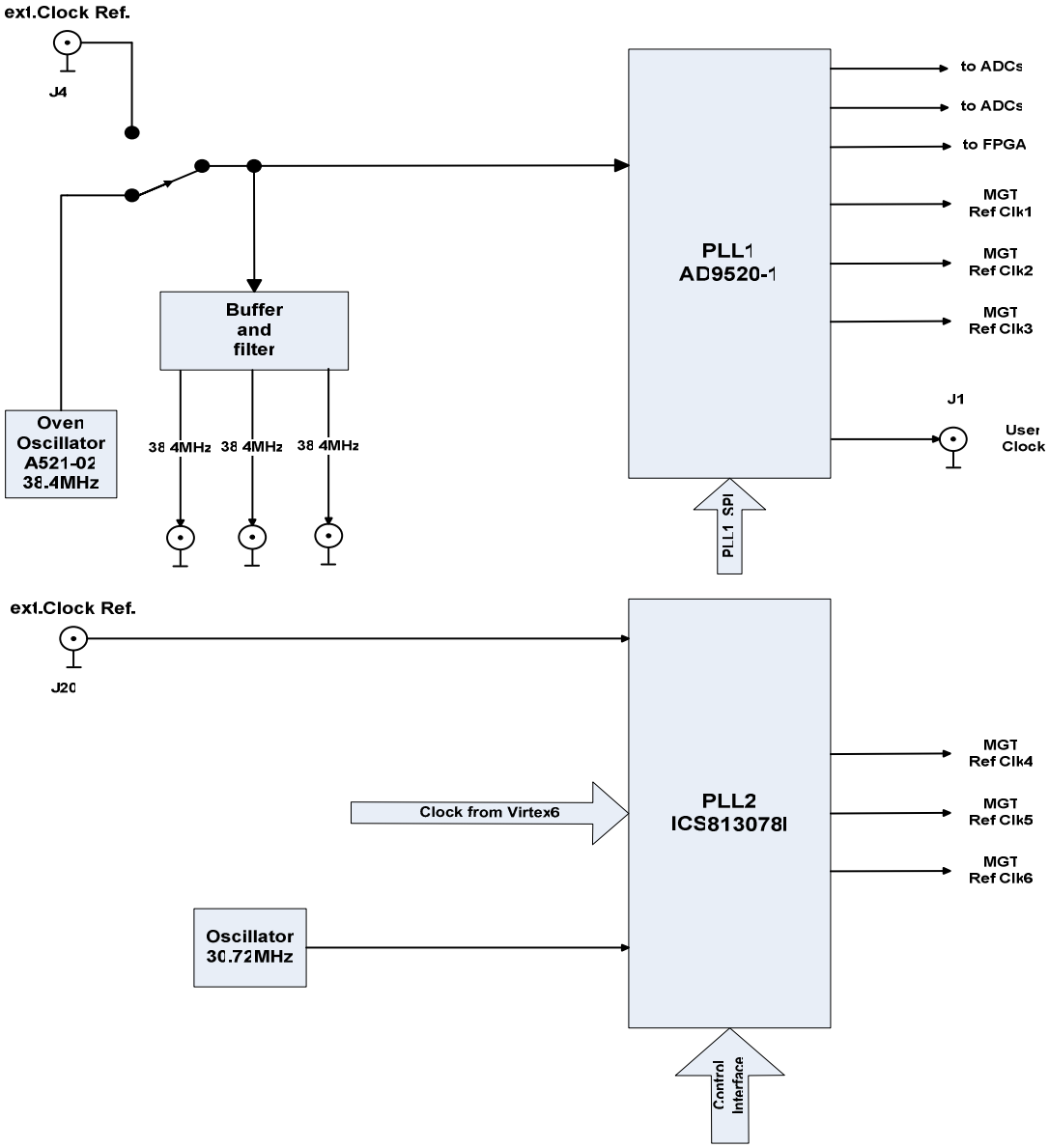


Figure 3: PLL's and clock distribution

4. Analog to digital conversion

The Virtex6 ADC board includes two double AD converters ADS62P49. Each converter has 14-Bit data interface and the maximal sampling rate is 250MS/s. The maximal analog input level is 2Vpp. The converters can be programmed from Virtex6 via SPI interface.

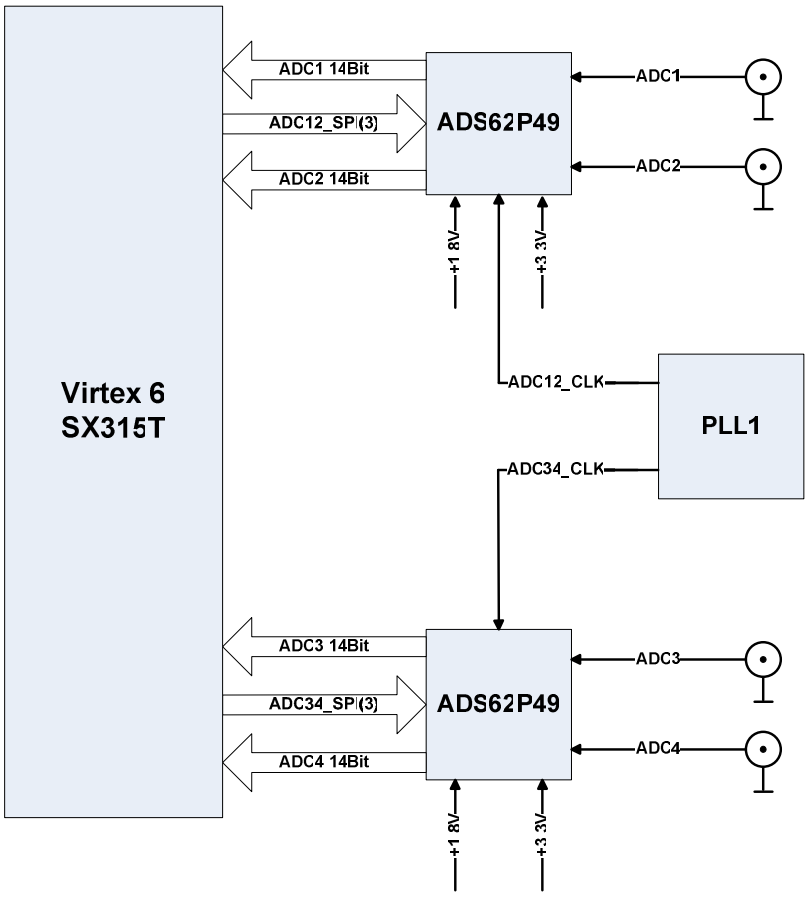


Figure 4: Analog to digital conversion

5. PCIexpress Interface

The PCIe interface includes 4 lanes and can be connected via cable to PC. The Xilinx PCIe core can use reference clock directly from PC or from on board oscillator X1 (100MHz). It is recommended to use a PC reference clock.

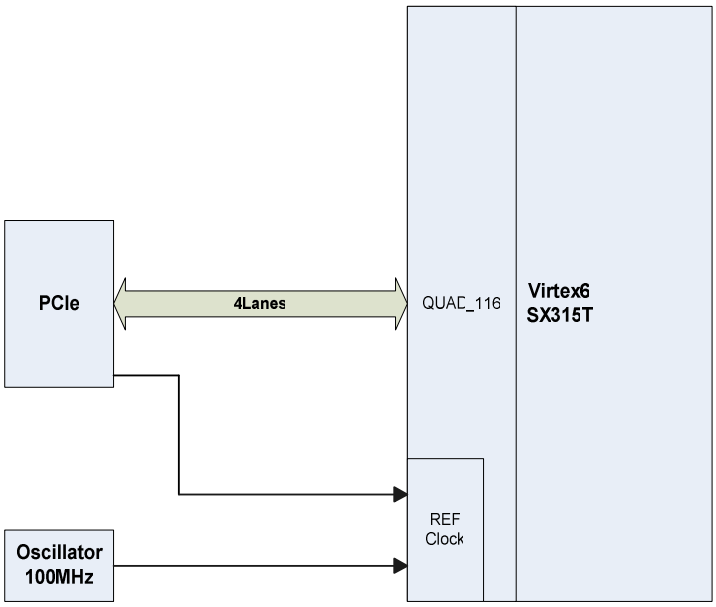


Figure 5: PCIExpress interface

6. SRIO Interface.

The SRIO interface includes 4 lanes and can be connected via cable to external hardware. The reference clock can be provided either from oscillator X5 (125MHz) or from PLL1 (U1).

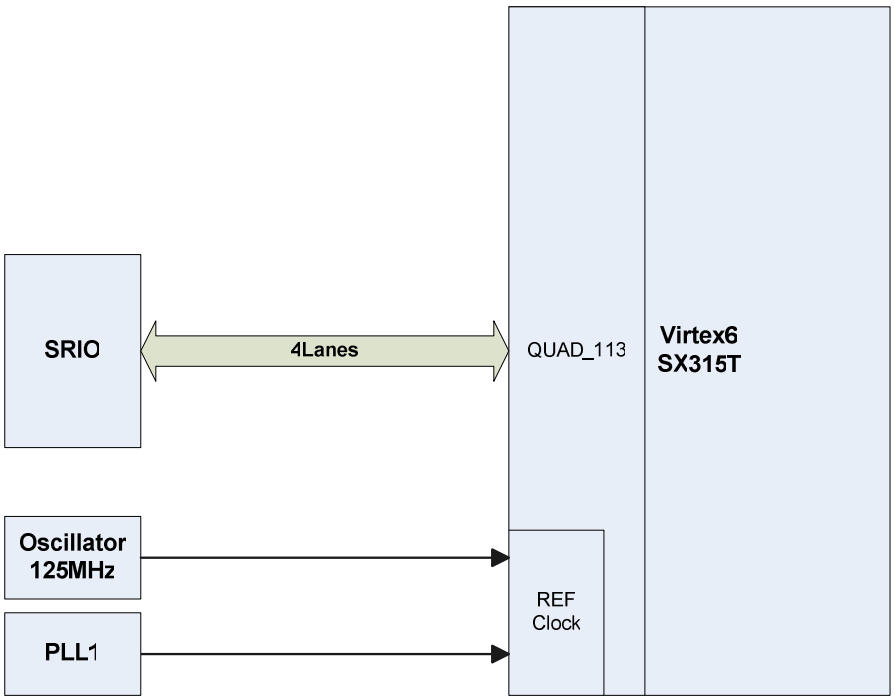


Figure 6: SRIO Interface

7. SATA Interface.

The SATA interface includes 2 SATA connectors and can be connected via cable to hard disc or another external hardware. The reference clock is provided either from oscillator X11 (150MHz) or from PLL2 (U21).

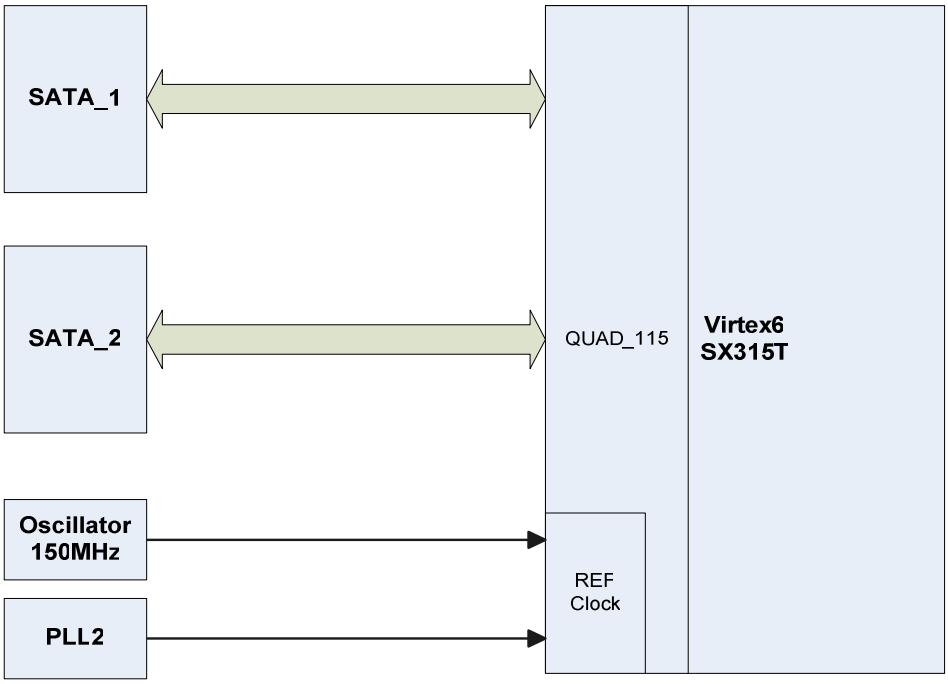


Figure 7: SATA Interface.

8. SFP interface.

The Virtex6 ADC board features eight SFP/SFP+ (Small Factor Pluggable) connectors for optical links (CPRI or OBSAI interfaces). The connectors are directly connected to high speed GTX modules of Virtex6 (Figure 8). The reference clocks can be generated in PLL1 (U1) or PLL2 (U21).

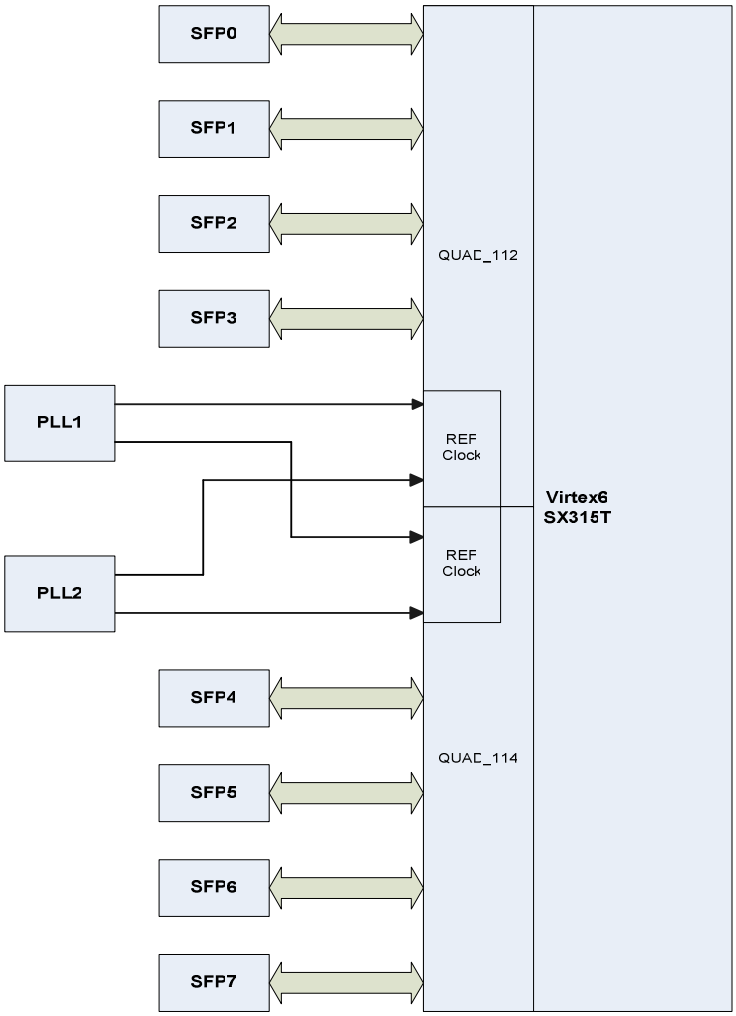


Figure 8: SFP interface

9. DDR3 Interface.

The DDR3 interface is developed for SODIMM modules up to 4GByte. The power supply voltage of DDR3 modules is 1.5V.

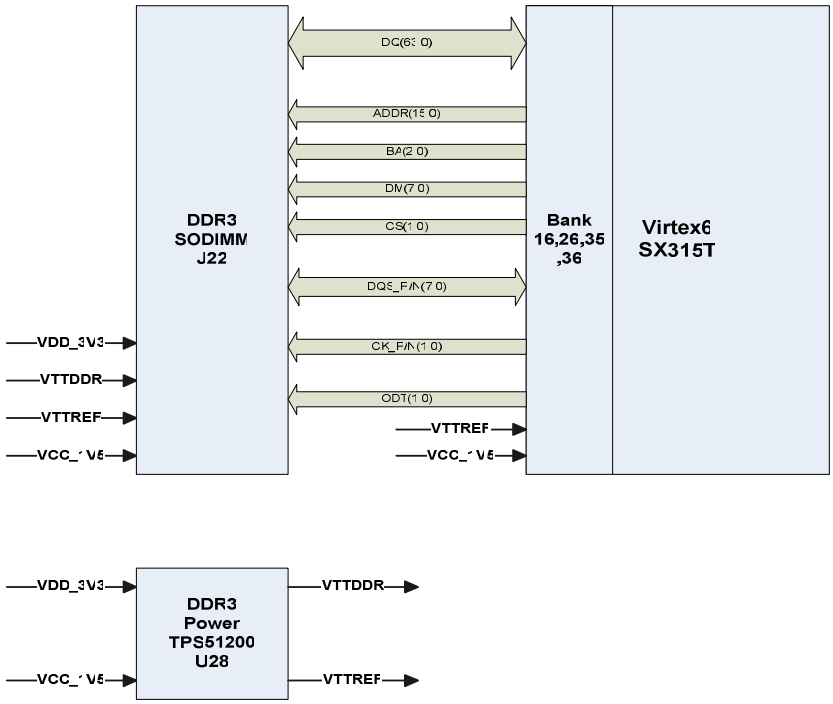


Figure 9: DDR3 Interface

10. Spartan 3AN.

The main function of Spartan FPGA is programming of Virtex 6 and external hardware via Ethernet. Spartan is used too for monitoring of board power consumption and temperature. The Spartan system included DDR2 interface, Ethernet, EEPROM , external FLASH and RS232 interface (see Figure 10).

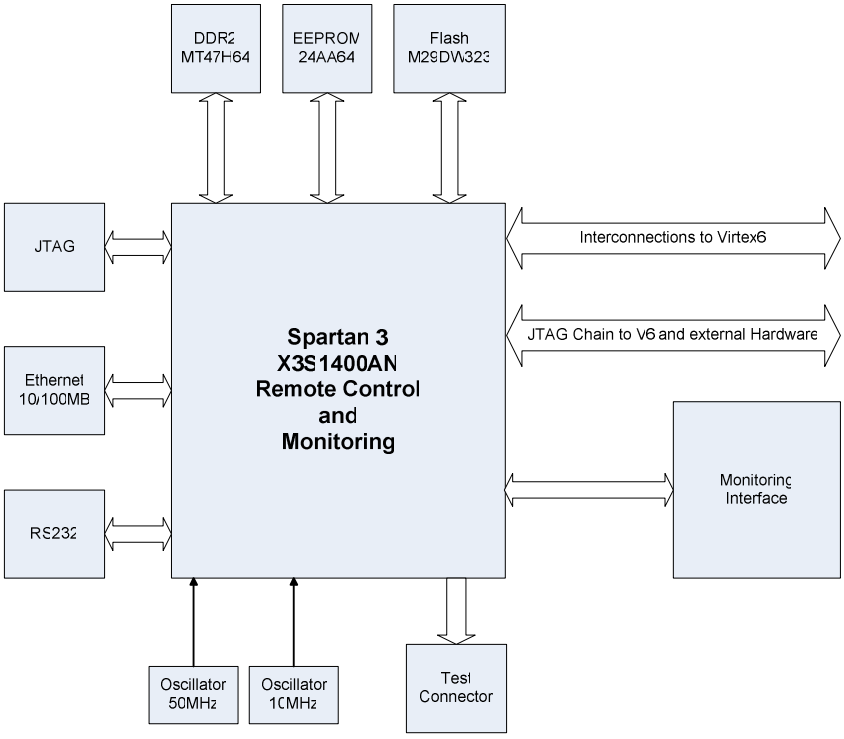


Figure 10: Spartan 3AN

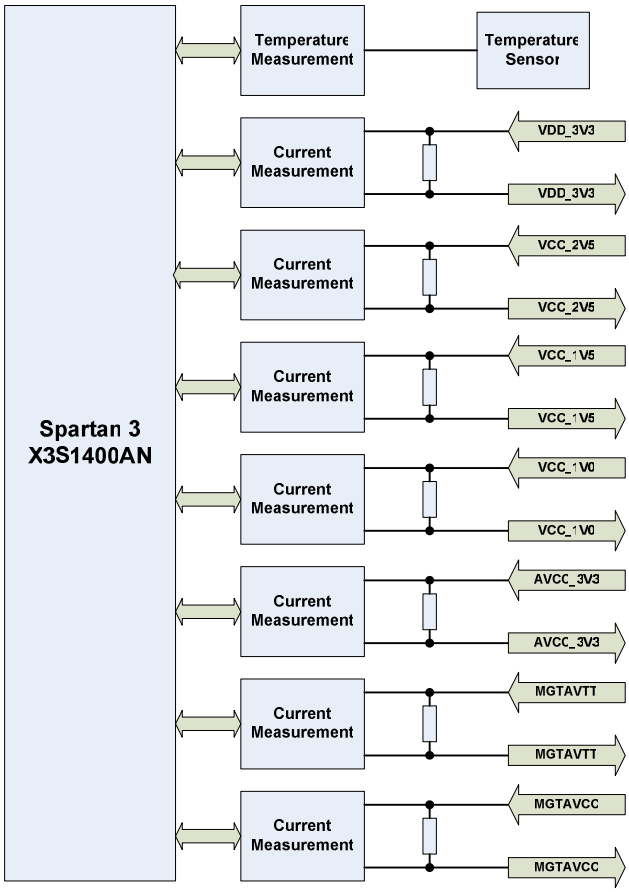


Figure 11: Temperature and current measurement

11. Interface to external Hardware.

The interface included three connectors (J16,J18 and J27). Each connector have 30 interconnections for free use and a JTAG interface for programming. The interface included power supply for external hardware. The voltage can be adjust in range 3.3V to 9V.

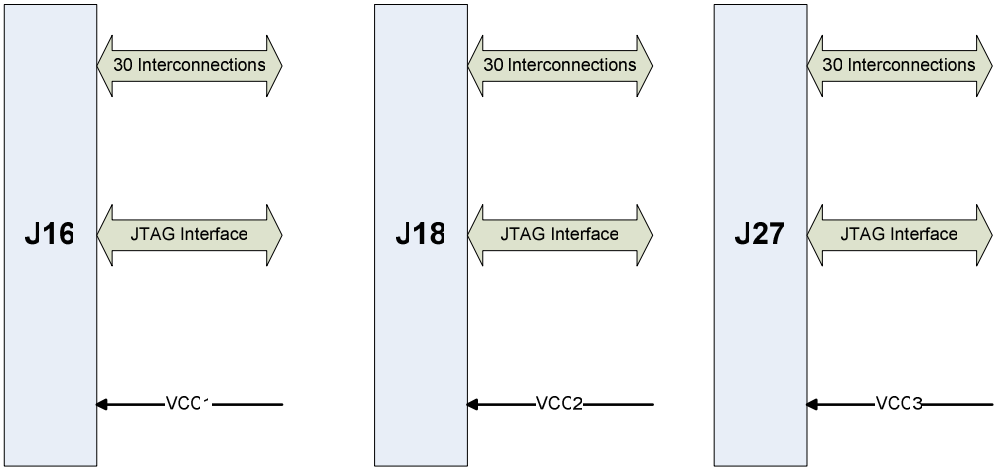


Figure 12: Interface to external Hardware

12. DC-Specification:

	Min	Typ	Max
Power Supply Voltage Range(+5V)	+4,5 V	+5 V	+5,5 V
Power Supply Current(+5V)		TBD	
Power Supply Voltage Range(+12V)	+11 V	+12 V	+13 V
Power Supply Current(+12V)		TBD	

13. Board Dimensions

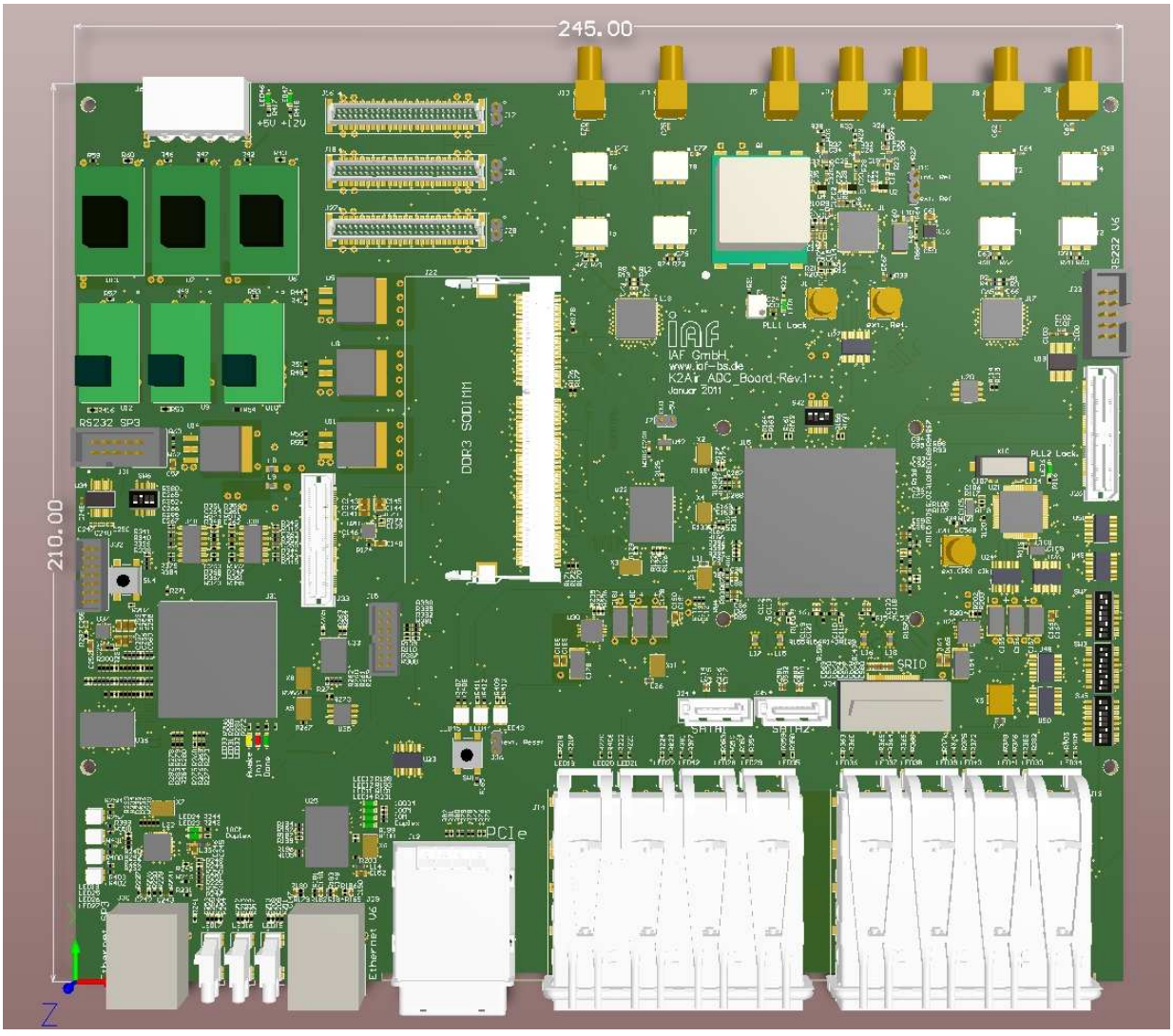


Figure 13: Board dimensions