

# Ethernet PHY – Board

## Data Sheet

Company: IAF GmbH  
Berliner Straße 52 J  
D-38104 Braunschweig  
Germany  
Phone: ++49 531 37988-0  
Fax: ++49 531 37988-30  
<http://www.iaf-bs.de>

Authors: Ronny Zavrtak  
Frank Luhn

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## 1 Introduction

The Ethernet PHY- Board is the physical layer device environment for the V4FX60-MAC-Board.

The module contains the following hardware components:

- 2x VCS8211
- 3x LED
- Ethernet Connector with integrated LEDs
- 64kbit I<sup>2</sup>C PROM
- 125 MHz Oscillator



Picture 1: top view

## 2 Hardware Description

One or two Ethernet PHY Chips can be used via Serial Gigabit Medium Independent Interface (SGMII) or parallel GMII. An additional Connector allows using MDIO to configure each PHY device. Configuration can also be done via resistors on the back side of the board or an optional EEPROM. The power supply can be taken from MAC Board.

picture 1: GMII/SGMII-Interface

### 2.1 Clock Generation

The clock generation section of the Board provides only a single ended 125 MHz clock for the VSC8211.

- User clock socket (Q1) 3.3V 125 MHz for GMII

For synchronization with the V4FX60 MAC Board a single ended Clock may be used via a MMXC Connector J8 (not recommended). R65 must be left open.

## 2.2 IIC-EEPROM

On the Ethernet PHY Board a serial 64kBit Electrically Erasable PROM (U2) is mounted. It supports a bi-directional 2-wire bus and data transmission protocol. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the START and STOP conditions, while the 24LC64 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. The WP pin allows the user to write protect the entire array (0000-1FFF) when the pin is tied to VCC. The Resistor R20 must be assigned to ground to enable EEPROM use.

## 2.3 Configuration CMODE 0-7

CMODE	3:0	Resistor value default
0	0000	0 to GND
1	1110	16,9k to VDD33A
2	1111	0 to VDD33A
3	1110	16,9k to VDD33A
4	1000	0 to VDD33A
5	0000	0 to GND
6	0001	2,26k to GND
7	1111	22,6k to VDD33A
Changed 3	0110	16,9k to gnd
Changed 4	0000	0 to gnd

table 1: resistor values

The CMODE register 0 and 1.2 are used to define the 5 bit address of the PHY device. Please refer to VSC8211 data sheet for more information.

## 2.4 LEDs

The Ethernet PHY Board provides 5 programmable LEDs that can be turned on by driving the LEDs signal high. Table 2 describes the user LEDs.

Signal Name	Pin Number	Description	IOSTANDARD	Direction
LED1	A13	LED 1 (yellow) TX/1000/Activity	LVC MOS33	O
LED2	B12	LED 2 (green) RX/1000/Activity	LVC MOS33	O
LED3	B13	LED 3 (red) TX	LVC MOS33	O
LED4	C12	LED 4 (yellow) Link	LVC MOS33	O
LED5	C13	LED 5 (green) RX/Activity	LVC MOS33	O

**Table 2: user LEDs pin assignment**

## **2.5 Reset**

The Reset can be done via MDIO connector (J19) pin5 (soft), pin6 (hard) or by writing into register 0 of the PHY chip.

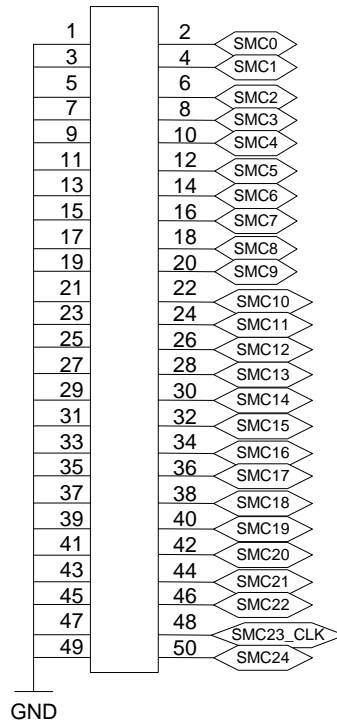
## **3 IO Connections**

The FX60 MAC Board is provided with different GPIO connectors which may fulfil various requirements. The included connectors are listed below:

- Extension Connectors (J2, J3) SAMTEC QSH-060-LDAK
- Motherboard Connectors (J30, J32) SAMTEC BKT-169
- Universal IO-Connector (J8) ERNI SMC-ML-Q 50V
- MDIO (J4) MOLEX 3 210620
- Universal Connector (J9) Molex 3 312020

### **3.1 Parallel IO Connector**

The picture below shows the connection of the ERNI SMC (J10, J17) connector. This connector can be used as general purpose interface but in particular it is designed for the use as Gigabit Medium Independent Interface (GMII). In this case pin assignment is as listed in Table 3.



**Picture 2: ERNI SMC**

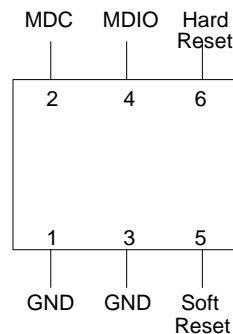
Signal Name	Description	IOSTANDARD	Direction
SMC0	pin2 (GMII TXD<0>)	LVCMOS33	O
SMC1	pin4 (GMII TXD<1>)	LVCMOS33	O
SMC2	pin6 (GMII TXD<2>)	LVCMOS33	O
SMC3	pin8 (GMII TXD<3>)	LVCMOS33	O
SMC4	pin10 (GMII TXD<4>)	LVCMOS33	O
SMC5	pin12 (GMII TXD<5>)	LVCMOS33	O
SMC6	pin14 (GMII TXD<6>)	LVCMOS33	O
SMC7	pin16 (GMII TXD<7>)	LVCMOS33	O
SMC8	pin18 (GMII TXEN)	LVCMOS33	O
SMC9	pin20 (GMII TXER)	LVCMOS33	O
SMC10	pin22 (GTX_CLK)	LVCMOS33	O
SMC11	pin24 (GMII RXD<0>)	LVCMOS33	I
SMC12	pin26 (GMII RXD<1>)	LVCMOS33	I
SMC13	pin28 (GMII RXD<2>)	LVCMOS33	I
SMC14	pin30 (GMII RXD<3>)	LVCMOS33	I
SMC15	pin32 (GMII RXD<4>)	LVCMOS33	I
SMC16	pin34 (GMII RXD<5>)	LVCMOS33	I
SMC17	pin36 (GMII RXD<6>)	LVCMOS33	I
SMC18	pin38 (GMII RXD<7>)	LVCMOS33	I

SMC19	pin40 (GMII RXDV)	LVC MOS33	I
SMC20	pin42 (GMII RXER)	LVC MOS33	I
SMC21	pin44 (GMII COL)	LVC MOS33	I
SMC22	pin46 (GMII CRS)	LVC MOS33	I
SMC23_Clk	pin48 (GMII RXCLK)	LVC MOS33	I
SMC24	pin50 (n.c.)	LVC MOS33	IO

**Table 3: SMC pin assignment**

### 3.2 Universal IO Connector (MDIO)

The Ethernet PHY Board provides a small MOLEX connector (J19) which is prepared for the use as Management Data In/ Out (MDIO). This allows sending configuration data to both of the Ethernet PHYs via one connection. Picture 8 shows the pin assignment of the MOLEX connector.



**Picture 3: MDIO MOLEX connector pin assignment**

Signal Name	Description	IOSTANDARD	Direction
Hard_Reset	J19 pin6 (MDIO-Connector)	LVC MOS33	IO
Soft_Reset	J19 pin5 (MDIO-Connector)	LVC MOS33	IO
MDIO_D	J19 pin4 (MDIO-Connector)	LVC MOS33	IO
MDIO_MDC	J19 pin2 (MDIO-Connector)	LVC MOS33	IO

**Table 4: MDIO MOLEX pin definition**

## 4 Mini MCX

The MMCX connectors (J13, J14, J15, J16, J17, J17, J18, J19) may be used to connect with the V4FX60 MAC Board. They are prepared for use with Serial GMII of the Virtex4 Ethernet MAC Hardmacro.