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## **Digital Signal Processor (DSP) Add-On Module (Rev. 1.0)**

(Data Sheet Rev. 1.0 October 2005)

The DSP-Module for the FFP-Basic-Board consists of two DSP-Add-On boards (Type A and Type B), which are designed for use on a single extension slot of the FFP-Basic board (see Figure 1 and Figure 2). Both boards have the same features and can also be used on different extension slots.

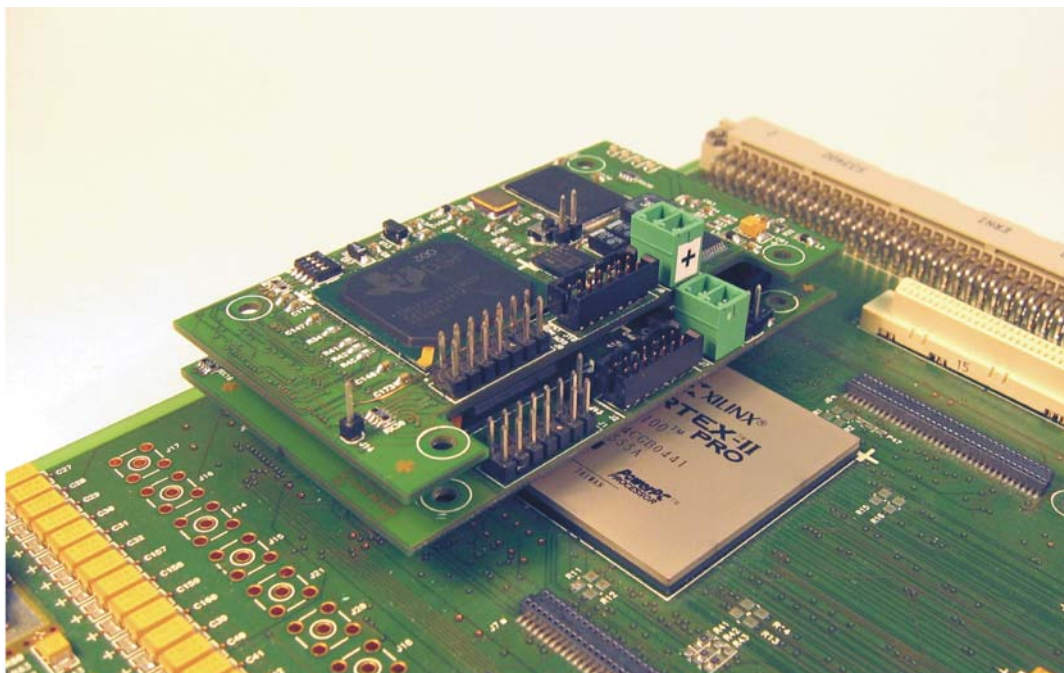


Figure 1: Two DSP-Add-On-Boards on one extension slot

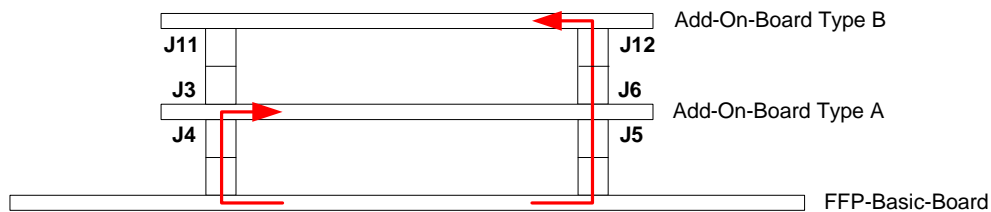


Figure 2: Use of the two DSP-Add-On-Boards on one slot of th FFP-Basic-Board

Each Add-On-Board has the following key features:

- Texas Instruments DSP TMS320C6713 operating at 300 MHz
- JTAG-Connector for use with an external emulator
- 2 MByte SRAM (divided into two blocks, with 2 SRAMs organized 256 k x 32 bit per block)
- 2 MByte Flash EPROM (1 M x 16 bit)
- CPLD (Reset- and LED-Control) with separat JTAG-Connector
- Interface for communication with the FFP-Basic-Board (Table 1 and 2)
- 4 Dip-Switches for DSP-Configuration (Table 4)
- 4 LEDs
- Connector for external power supply (+3,3 V)

#### DC-Specification:

	Min	Typ	Max
Power Supply Voltage Range:	+3.13 V	+3.3 V	+3.47 V
Power Supply Current:	-	0.5 A	-

**Block Diagramm:**

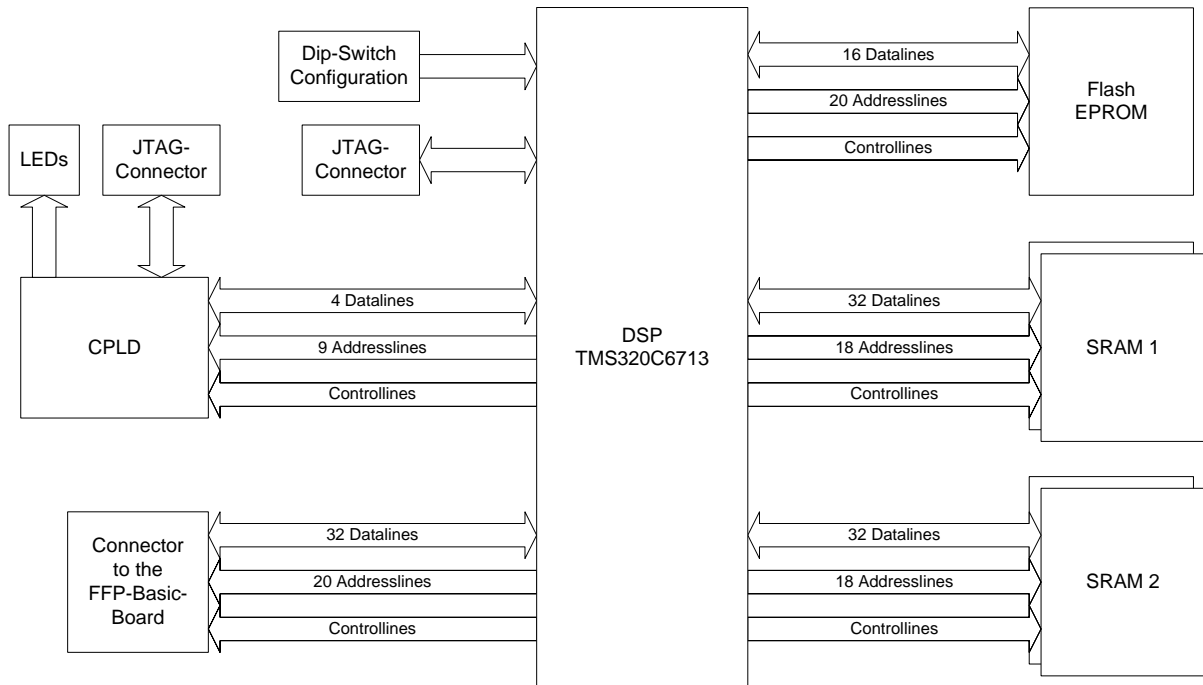


Figure 3: Block Diagramm DSP-Add-On-Board

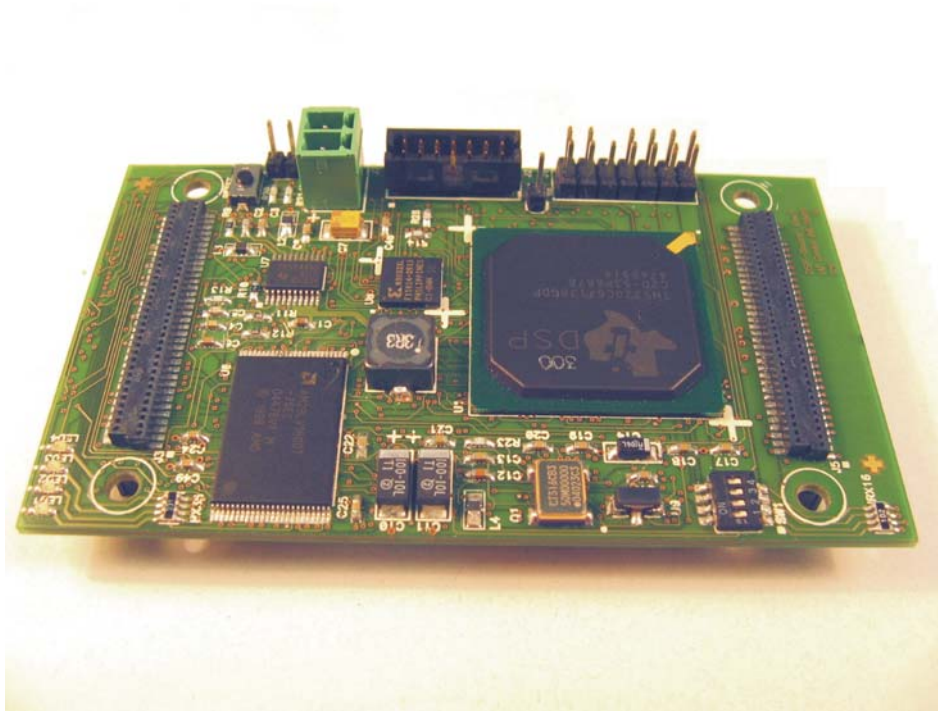


Figure 4: DSP-Add-On-Board Type A

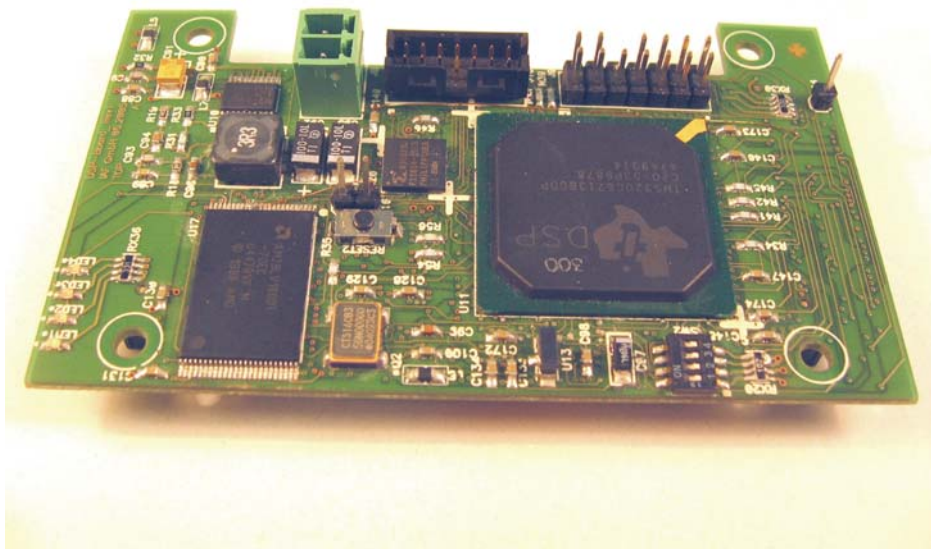


Figure 5: DSP-Add-On-Board Type B

**Board -Dimensions:** 54 mm x 90 mm

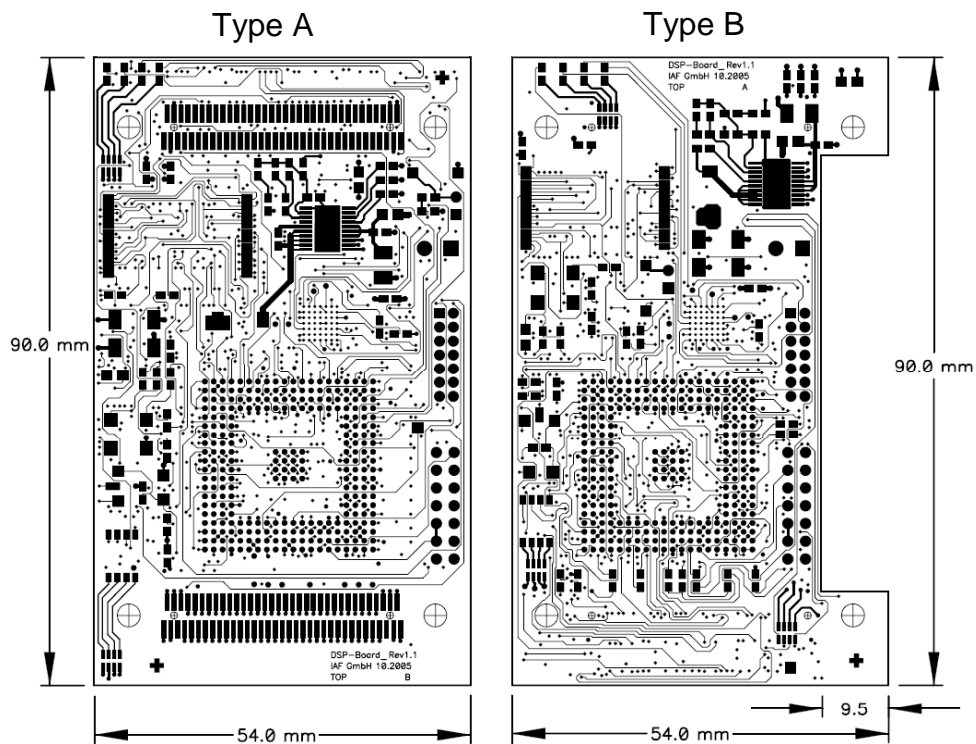


Figure 6: DSP-Add-On-Boards (Type A and B) – Board Dimensions

**Pinout of FFP-Connectors:**

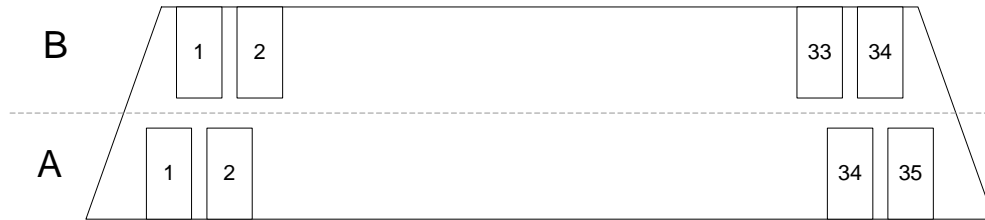


Figure 7: Schematic of the Connectors to the FFP-Basic-Board

Table 1: Pinout of the Connectors on the Add-On-Board Type A (J4)

Pin Name	Signal Description	Signal Type	Pin Name	Signal Description	Signal Type
A1	ECLKOUT	Output	B1	Data_Bus_0	Output/Input
A2	GND		B2	GND	
A3	Not Connected		B3	Data_Bus_1	Output/Input
A4	Address_Bus_0	Output	B4	Data_Bus_2	Output/Input
A5	Address_Bus_1	Output	B5	Data_Bus_3	Output/Input
A6	Address_Bus_2	Output	B6	Data_Bus_4	Output/Input
A7	Address_Bus_3	Output	B7	Data_Bus_5	Output/Input
A8	Address_Bus_4	Output	B8	Data_Bus_6	Output/Input
A9	Address_Bus_5	Output	B9	Data_Bus_7	Output/Input
A10	Address_Bus_6	Output	B10	Data_Bus_8	Output/Input
A11	Address_Bus_7	Output	B11	Data_Bus_9	Output/Input
A12	Address_Bus_8	Output	B12	Data_Bus_10	Output/Input
A13	Address_Bus_9	Output	B13	Data_Bus_11	Output/Input
A14	Address_Bus_10	Output	B14	Data_Bus_12	Output/Input
A15	Address_Bus_11	Output	B15	Data_Bus_13	Output/Input
A16	Address_Bus_12	Output	B16	Data_Bus_14	Output/Input
A17	Address_Bus_13	Output	B17	Data_Bus_15	Output/Input
A18	Address_Bus_14	Output	B18	Data_Bus_16	Output/Input
A19	Address_Bus_15	Output	B19	Data_Bus_17	Output/Input
A20	Address_Bus_16	Output	B20	Data_Bus_18	Output/Input
A21	Address_Bus_17	Output	B21	Data_Bus_19	Output/Input
A22	Address_Bus_18	Output	B22	Data_Bus_20	Output/Input
A23	Address_Bus_19	Output	B23	Data_Bus_21	Output/Input
A24	CE0	Output	B24	Data_Bus_22	Output/Input
A25	ARE	Output	B25	Data_Bus_23	Output/Input
A26	AOE	Output	B26	Data_Bus_24	Output/Input
A27	AWE	Output	B27	Data_Bus_25	Output/Input
A28	CPLD_0	Output/Input	B28	Data_Bus_26	Output/Input
A29	CPLD_1	Output/Input	B29	Data_Bus_27	Output/Input
A30	CPLD_2	Output/Input	B30	Data_Bus_28	Output/Input
A31	NMI	Input	B31	Data_Bus_29	Output/Input

A32	EXTReset	Input	B32	Data_Bus_30	Output/Input
A33	Not Connected		B33	GND	
A34	GND		B34	ECLKOUT_2	Output
A35	Data_Bus_31	Output/Input	-	-	

Table 2: Pinout of the Connectors on the Add-On-Board Type B (J12)

Pin Name	Signal Description	Signal Type	Pin Name	Signal Description	Signal Type
A1	Not Connected		B1	Data_Bus_0_2	Output/Input
A2	GND		B2	GND	
A3	Not Connected		B3	Data_Bus_1_2	Output/Input
A4	Address_Bus_0_2	Output	B4	Data_Bus_2_2	Output/Input
A5	Address_Bus_1_2	Output	B5	Data_Bus_3_2	Output/Input
A6	Address_Bus_2_2	Output	B6	Data_Bus_4_2	Output/Input
A7	Address_Bus_3_2	Output	B7	Data_Bus_5_2	Output/Input
A8	Address_Bus_4_2	Output	B8	Data_Bus_6_2	Output/Input
A9	Address_Bus_5_2	Output	B9	Data_Bus_7_2	Output/Input
A10	Address_Bus_6_2	Output	B10	Data_Bus_8_2	Output/Input
A11	Address_Bus_7_2	Output	B11	Data_Bus_9_2	Output/Input
A12	Address_Bus_8_2	Output	B12	Data_Bus_10_2	Output/Input
A13	Address_Bus_9_2	Output	B13	Data_Bus_11_2	Output/Input
A14	Address_Bus_10_2	Output	B14	Data_Bus_12_2	Output/Input
A15	Address_Bus_11_2	Output	B15	Data_Bus_13_2	Output/Input
A16	Address_Bus_12_2	Output	B16	Data_Bus_14_2	Output/Input
A17	Address_Bus_13_2	Output	B17	Data_Bus_15_2	Output/Input
A18	Address_Bus_14_2	Output	B18	Data_Bus_16_2	Output/Input
A19	Address_Bus_15_2	Output	B19	Data_Bus_17_2	Output/Input
A20	Address_Bus_16_2	Output	B20	Data_Bus_18_2	Output/Input
A21	Address_Bus_17_2	Output	B21	Data_Bus_19_2	Output/Input
A22	Address_Bus_18_2	Output	B22	Data_Bus_20_2	Output/Input
A23	Address_Bus_19_2	Output	B23	Data_Bus_21_2	Output/Input
A24	CE0_2	Output	B24	Data_Bus_22_2	Output/Input
A25	ARE_2	Output	B25	Data_Bus_23_2	Output/Input
A26	AOE_2	Output	B26	Data_Bus_24_2	Output/Input
A27	AWE_2	Output	B27	Data_Bus_25_2	Output/Input
A28	CPLD_0_2	Output/Input	B28	Data_Bus_26_2	Output/Input
A29	CPLD_1_2	Output/Input	B29	Data_Bus_27_2	Output/Input
A30	CPLD_2_2	Output/Input	B30	Data_Bus_28_2	Output/Input
A31	NMI_2	Input	B31	Data_Bus_29_2	Output/Input
A32	EXT_Reset_2	Input	B32	Data_Bus_30_2	Output/Input
A33	Not Connected		B33	GND	
A34	GND		B34	Not Connected	
A35	Data_Bus_31_2	Output/Input	-	-	

## Signal Description

Table 3: Signal Description

Signal Name	Signals Description
ECLKOUT / ECLKOUT_2	Output Clock of the DSP
CE0 / CE0_2	Chip Enable Signal from DSP to FFP-Basic-Board
ARE / ARE_2	Asynchron-Read-Enable Signal from DSP to FFP-Basic-Board
AOE / AOE_2	Asynchron-Output-Enable from DSP to FFP-Basic-Board
AWE / AWE_2	Asynchron-Write-Enable from DSP to FFP-Basic-Board
CPLD_0 / CPLD_0_2	Free useable Connection between CPLD and FFP-Basic-Board
CPLD_1 / CPLD_1_2	Free useable Connection between CPLD and FFP-Basic-Board
CPLD_2 / CPLD_2_2	Free useable Connection between CPLD and FFP-Basic-Board
NMI / NMI_2	Non Maskable Interrupt from FFP-Basic-Board to DSP
EXT_Reset / EXT_Reset_2	Reset from FFP-Basic-Board to DSP
Address_Bus_0 to 19 Address_Bus_0_2 to 19_2	20 bit Address Bus from DSP to FFP-Basic-Board
Data_Bus_0 to 31 Data_Bus_0_2 to 31_2	32 bit Data Bus between DSP and FFP-Basic-Board

## DSP-Configuration:

Table 4: Dip-Switch-Setting for DSP-Configuration

Switch1	Switch2	Switch3	Switch4	Configuration Description
Off	Off			8-bit-ROM-Boot
Off	On			Host/Emulation Boot (not useable)
On	Off			32-bit-ROM-Boot (not useable)
On	On			16-bit-ROM-Boot
		Off		Little Endian
		On		Big Endian
			Off	Data is always present on the ED[7:0] side off the bus
			On	In <i>Little Endian mode</i> the 8-bit or 16-bit EMIF data will be present on the ED[7:0] side of the bus. In <i>Big Endian mode</i> the 8-bit or 16-bit EMIF data will be present on the ED[31:24] side of the bus.

## **Integrated Devices**

**TMS320C6713** DSP from Texas Instruments

Datasheet: <http://focus.ti.com/lit/ds/symlink/tms320c6713.pdf>

**IDT71V416L** SRAM from IDT

Datasheet: <http://www1.idt.com/pcms/tempDocs/71V416ds.pdf>

**Am29LV160D** Flash EPROM from AMD

Datasheet: [http://www.amd.com/us-en/assets/content\\_type/white\\_papers\\_and\\_tech\\_docs/am29lv400b.pdf](http://www.amd.com/us-en/assets/content_type/white_papers_and_tech_docs/am29lv400b.pdf)

**XCR3032XL** CPLD from Xilinx

Family-Datasheet: <http://direct.xilinx.com/bvdocs/publications/ds012.pdf>

Datasheet: <http://direct.xilinx.com/bvdocs/publications/ds023.pdf>