

IAF GmbH
Berliner Straße 52j
38104 Braunschweig
Germany

Phone.: ++49 531 379 88-0
Fax: ++49 531 37988-30
e-mail: info@iaf-bs.de
www.iaf-bs.de

LVDS Interface Board (Rev. 1.0)

(Data Sheet Rev. 1.0 March 2004)

Low-Voltage Differential Signalling (LVDS) allows a fast and reliable data transfer. It is easy to use and fail safe, for the drivers are protected against open circuit and short circuit. The LVDS Interface Board is constructed as an add-on board for the following FPGA platforms:

- *iaf FFP Basic*
- *prodesign CHIPit Gold Edition*.

For connecting the FPGA board via LVDS to a PC, a fitting High Speed PCI Card is available.

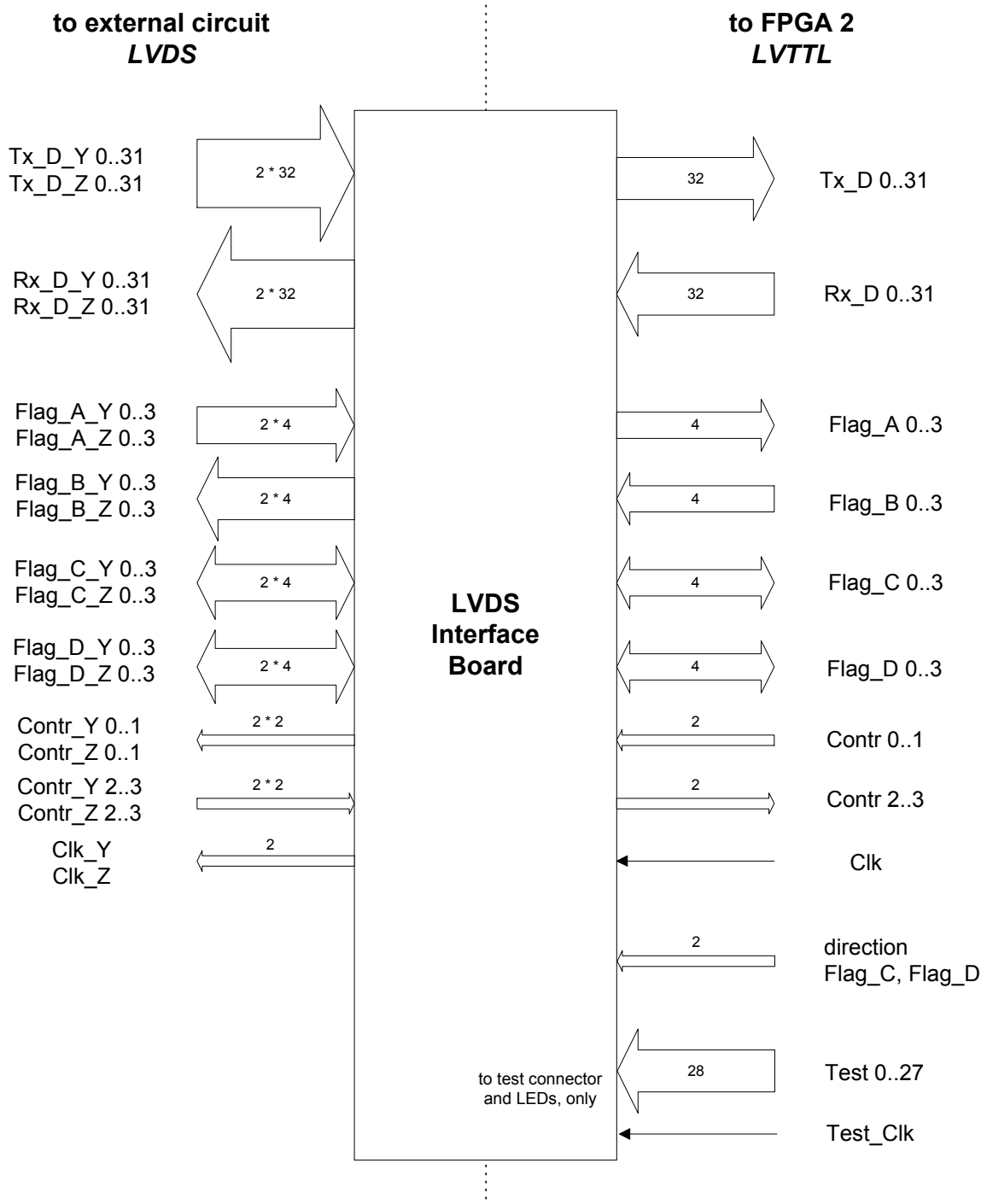


The LVDS Interface Board provides an 80bit parallel interface with additional clock and control lines. An overview is given in the figure below. The LVDS interface is connected via three 68pin Mini-SUB-D connectors (female). So, for example, SCSI2-cables may be used, which are easily available as PC accessory. The integrated termination resistors are designed for a line impedance of about 100Ω.

All connections to the FPGA board are accessible via test connectors. Furthermore the interface board provides 27 additional measurement pins equipped with a separate clock line. The measurement pins can be expanded to 32 bit, if FLAG_D0..3 are not used. The status of the 8 lower test pins is indicated by LEDs. All test connectors are compatible to the *Agilent High Density Probe Adapter E5385A*. The LVDS Interface Board is supplied by the FPGA board via the 3.3V pins of the extension slot.

Note: For mechanical reasons the LVDS Interface Board must be mounted at extension slot EB1 or EB4 of the board *iaf FFP Basic* respectively on EB4 of the board *prodesign CHIPit Gold Edition*!

Block diagram of LVDS Interface Board



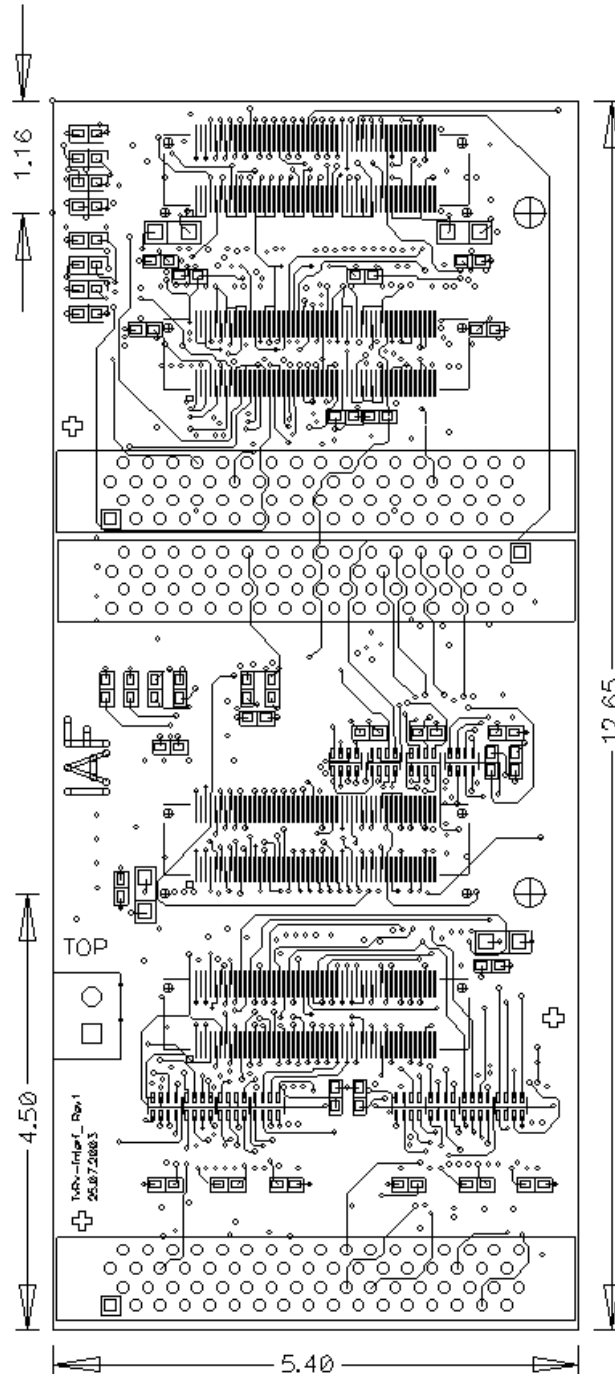
Note:

The direction of *Flag_C 0..3* and *Flag_D 0..3* is switchable by the FPGA. The direction of *Tx_D 0..31*, *Rx_D 0..31*, *Flag_A 0..3* or *Flag_B 0..3* can easily be changed by small hardware modifications.

Appendix

- Mechanical Dimensions
- Key Data of the used Devices
- Pinning of LVDS Interface
- Pinning at Extension Slot of FPGA Board
- Pinning of Probe Connectors for Logic Analyser
- LEDs

Mechanical Dimensions



Key Data of the used Devices

outgoing LVDS signals (Rx_D, Contr0..1, Flags):

- differential mode voltage $|V_{OD}| = 247 \dots 454\text{mV}$
- propagation delay 1.3 ... 3.6ns

incoming LVDS signals (Tx_D, Contr2..3, Flags, CLK):

- differential mode voltage $|V_{ID}| = 100 \dots 600\text{mV}$
- common voltage $V_{IC} = 0.5 * |V_{ID}| \dots 2.4\text{V} - 0.5 * |V_{ID}|$
- propagation delay 1 ... 4.5ns
- termination 88 ... 132 Ω

Note:

absolute maximum ratings,

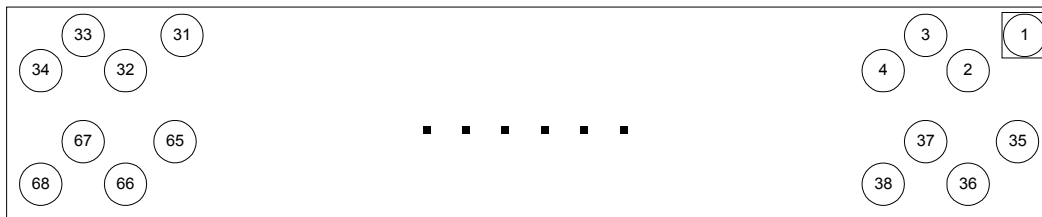
specification for load 50 Ω ||10pF (Rx_D, Flags) resp. 100 Ω ||10pF (Contr0..1)

Pinning of LVDS Interface

Basic parameters:

- connector: mini-SUB-D, 68 pin, female (cables must be fitted with male connectors), pinning see figure below
- ...Y: non-inverted pin of LVDS signal; ...Z: inverted pin

Pinning SUB-D; Component Side



Connector J8: Tx_D

<i>connector pin</i>	<i>wire no.</i>	<i>signal</i>	<i>connector pin</i>	<i>wire no.</i>	<i>signal</i>
1	1	GND	18	35	Tx_D_Y16
35	2	GND	52	36	Tx_D_Z16
2	3	Tx_D_Y0	19	37	Tx_D_Y17
36	4	Tx_D_Z0	53	38	Tx_D_Z17
3	5	Tx_D_Y1	20	39	Tx_D_Y18
37	6	Tx_D_Z1	54	40	Tx_D_Z18
4	7	Tx_D_Y2	21	41	Tx_D_Y19
38	8	Tx_D_Z2	55	42	Tx_D_Z19
5	9	Tx_D_Y3	22	43	Tx_D_Y20
39	10	Tx_D_Z3	56	44	Tx_D_Z20
6	11	Tx_D_Y4	23	45	Tx_D_Y21
40	12	Tx_D_Z4	57	46	Tx_D_Z21
7	13	Tx_D_Y5	24	47	Tx_D_Y22
41	14	Tx_D_Z5	58	48	Tx_D_Z22
8	15	Tx_D_Y6	25	49	Tx_D_Y23
42	16	Tx_D_Z6	59	50	Tx_D_Z23
9	17	Tx_D_Y7	26	51	Tx_D_Y24
43	18	Tx_D_Z7	60	52	Tx_D_Z24
10	19	Tx_D_Y8	27	53	Tx_D_Y25
44	20	Tx_D_Z8	61	54	Tx_D_Z25
11	21	Tx_D_Y9	28	55	Tx_D_Y26
45	22	Tx_D_Z9	62	56	Tx_D_Z26
12	23	Tx_D_Y10	29	57	Tx_D_Y27
46	24	Tx_D_Z10	63	58	Tx_D_Z27
13	25	Tx_D_Y11	30	59	Tx_D_Y28
47	26	Tx_D_Z11	64	60	Tx_D_Z28
14	27	Tx_D_Y12	31	61	Tx_D_Y29
48	28	Tx_D_Z12	65	62	Tx_D_Z29
15	29	Tx_D_Y13	32	63	Tx_D_Y30
49	30	Tx_D_Z13	66	64	Tx_D_Z30
16	31	Tx_D_Y14	33	65	Tx_D_Y31
50	32	Tx_D_Z14	67	66	Tx_D_Z31
17	33	Tx_D_Y15	34	67	GND
51	34	Tx_D_Z15	68	68	GND

Connector J7: Rx_D

<i>connector pin</i>	<i>wire no.</i>	<i>signal</i>	<i>connector pin</i>	<i>wire no.</i>	<i>signal</i>
1	1	GND	18	35	Rx_D_Y16
35	2	GND	52	36	Rx_D_Z16
2	3	Rx_D_Y0	19	37	Rx_D_Y17
36	4	Rx_D_Z0	53	38	Rx_D_Z17
3	5	Rx_D_Y1	20	39	Rx_D_Y18
37	6	Rx_D_Z1	54	40	Rx_D_Z18
4	7	Rx_D_Y2	21	41	Rx_D_Y19
38	8	Rx_D_Z2	55	42	Rx_D_Z19
5	9	Rx_D_Y3	22	43	Rx_D_Y20
39	10	Rx_D_Z3	56	44	Rx_D_Z20
6	11	Rx_D_Y4	23	45	Rx_D_Y21
40	12	Rx_D_Z4	57	46	Rx_D_Z21
7	13	Rx_D_Y5	24	47	Rx_D_Y22
41	14	Rx_D_Z5	58	48	Rx_D_Z22
8	15	Rx_D_Y6	25	49	Rx_D_Y23
42	16	Rx_D_Z6	59	50	Rx_D_Z23
9	17	Rx_D_Y7	26	51	Rx_D_Y24
43	18	Rx_D_Z7	60	52	Rx_D_Z24
10	19	Rx_D_Y8	27	53	Rx_D_Y25
44	20	Rx_D_Z8	61	54	Rx_D_Z25
11	21	Rx_D_Y9	28	55	Rx_D_Y26
45	22	Rx_D_Z9	62	56	Rx_D_Z26
12	23	Rx_D_Y10	29	57	Rx_D_Y27
46	24	Rx_D_Z10	63	58	Rx_D_Z27
13	25	Rx_D_Y11	30	59	Rx_D_Y28
47	26	Rx_D_Z11	64	60	Rx_D_Z28
14	27	Rx_D_Y12	31	61	Rx_D_Y29
48	28	Rx_D_Z12	65	62	Rx_D_Z29
15	29	Rx_D_Y13	32	63	Rx_D_Y30
49	30	Rx_D_Z13	66	64	Rx_D_Z30
16	31	Rx_D_Y14	33	65	Rx_D_Y31
50	32	Rx_D_Z14	67	66	Rx_D_Z31
17	33	Rx_D_Y15	34	67	GND
51	34	Rx_D_Z15	68	68	GND

Connector J9: Flags, Clock and Control

<i>connector pin</i>	<i>wire no.</i>	<i>signal</i>	<i>connector pin</i>	<i>wire no.</i>	<i>signal</i>
1	1	GND	18	35	CONTR1_Y
35	2	GND	52	36	CONTR1_Z
2	3	Flag_A_Y0	19	37	CONTR0_Y
36	4	Flag_A_Z0	53	38	CONTR0_Z
3	5	Flag_A_Y1	20	39	CONTR2_Y
37	6	Flag_A_Z1	54	40	CONTR2_Z
4	7	Flag_A_Y2	21	41	CONTR3_Y
38	8	Flag_A_Z2	55	42	CONTR3_Z
5	9	Flag_A_Y3	22	43	GND
39	10	Flag_A_Z3	56	44	GND
6	11	Flag_B_Y0	23	45	CLK_Y
40	12	Flag_B_Z0	57	46	CLK_Z
7	13	Flag_B_Y1	24	47	GND
41	14	Flag_B_Z1	58	48	GND
8	15	Flag_B_Y2	25	49	GND
42	16	Flag_B_Z2	59	50	GND
9	17	Flag_B_Y3	26	51	GND
43	18	Flag_B_Z3	60	52	GND
10	19	Flag_C_Y0	27	53	GND
44	20	Flag_C_Z0	61	54	GND
11	21	Flag_C_Y1	28	55	GND
45	22	Flag_C_Z1	62	56	GND
12	23	Flag_C_Y2	29	57	GND
46	24	Flag_C_Z2	63	58	GND
13	25	Flag_C_Y3	30	59	GND
47	26	Flag_C_Z3	64	60	GND
14	27	Flag_D_Y0	31	61	GND
48	28	Flag_D_Z0	65	62	GND
15	29	Flag_D_Y1	32	63	GND
49	30	Flag_D_Z1	66	64	GND
16	31	Flag_D_Y2	33	65	GND
50	32	Flag_D_Z2	67	66	GND
17	33	Flag_D_Y3	34	67	GND
51	34	Flag_D_Z3	68	68	GND

Pinning at Extension Slot of FPGA Board

Interface EB4				
Row	Connector A		Connector B	
	A-Part	B-Part	A-Part	B-Part
1	Rx_D0	Rx_D29	VRP_Bank5 **	VRN_BANK5 **
2	GND	GND	GND	GND
3	VCC	VRP_Bank0 **	VCC	Tx_D29
4	Rx_D1	Rx_D30	Tx_D0	Tx_D30
5	VRN_Bank0 **	Rx_D31	Tx_D1	Tx_D31
6	Rx_D2	Test0	Tx_D2	Flag_A0
7	Rx_D3	VRN_Bank7 **	Tx_D3	Flag_A1
8	Rx_D4	Test1	Tx_D4	VRP_Bank6 **
9	VRP_Bank7 **	Test2	VRN_Bank6 **	Flag_A2
10	Rx_D5	Test3	Tx_D5	Flag_A3
11	Rx_D6	Test4	Tx_D6	Flag_B0
12	Rx_D7	Test5	Tx_D7	Flag_B1
13	Rx_D8	Test6	Tx_D8	Flag_B2
14	Rx_D9	Test7	Tx_D9	Flag_B3
15	Rx_D10	Test8	Tx_D10	Flag_C0
16	Rx_D11	Test9	Tx_D11	Flag_C1
17	Rx_D12	Test10	Tx_D12	Flag_C2
18	Rx_D13	Test11	Tx_D13	Flag_C3
19	Rx_D14	Test12	Tx_D14	Flag_D0 (Test28)*
20	Rx_D15	Test13	Tx_D15	Flag_D1 (Test29)*
21	Rx_D16	Test14	Tx_D16	Flag_D2 (Test30)*
22	Rx_D17	Test15	Tx_D17	Flag_D3 (Test31)*
23	Rx_D18	Test16	Tx_D18	Contr0
24	Rx_D19	Test17	Tx_D19	Contr1
25	Rx_D20	Test18	Tx_D20	Contr2
26	Rx_D21	Test19	Tx_D21	Contr3
27	Rx_D22	Test20	Tx_D22	Test25
28	Rx_D23	Test21	Tx_D23	Test26
29	Rx_D24	Test22	Tx_D24	Test27
30	Rx_D25	Test23	Tx_D25	Direction_Flag_C ***
31	Rx_D26	Test24	Tx_D26	Direction_Flag_D ***
32	Rx_D27	V5P	Tx_D27	V5P
33	VCC	GND	VCC	GND
34	GND	Test_CLK	GND	CLK
35	Rx_D28	rsvd	Tx_D28	rsvd

* The pins FLAG_D0..3 can alternatively be connected to TEST28..31 of Probe Connector J6.

** connected to the Digital Impedance Control (DCI) inputs of FPGA2 (for FPGA board Chiplt Gold, only); set to 50Ω.

*** direction of FLAG_C0...3 resp. FLAG_D0...3 (switchable by FPGA2);

high => LVDS output (same direction as Rx_D); low => LVDS input (same direction as Tx_D)

Pinning of Probe Connector J3 (Tx_D) for Logic Analyser

<i>pin no.</i>	<i>signal</i>	<i>pin name (Agilent probe)</i>	<i>pin no.</i>	<i>signal</i>	<i>pin name (Agilent probe)</i>
1	GND	GND	2	GND	GND
3	NC	NC	4	NC	NC
5	GND	GND	6	GND	GND
7	TX_D0	O_D0	8	TX_D16	E_D0
9	GND	GND	10	GND	GND
11	TX_D1	O_D1	12	TX_D17	E_D1
13	GND	GND	14	GND	GND
15	TX_D2	O_D2	16	TX_D18	E_D2
17	GND	GND	18	GND	GND
19	TX_D3	O_D3	20	TX_D19	E_D3
21	GND	GND	22	GND	GND
23	TX_D4	O_D4	24	TX_D20	E_D4
25	GND	GND	26	GND	GND
27	TX_D5	O_D5	28	TX_D21	E_D5
29	GND	GND	30	GND	GND
31	TX_D6	O_D6	32	TX_D22	E_D6
33	GND	GND	34	GND	GND
35	TX_D7	O_D7	36	TX_D23	E_D7
37	GND	GND	38	GND	GND
39	TX_D8	O_D8	40	TX_D24	E_D8
41	GND	GND	42	GND	GND
43	TX_D9	O_D9	44	TX_D25	E_D9
45	GND	GND	46	GND	GND
47	TX_D10	O_D10	48	TX_D26	E_D10
49	GND	GND	50	GND	GND
51	TX_D11	O_D11	52	TX_D27	E_D11
53	GND	GND	54	GND	GND
55	TX_D12	O_D12	56	TX_D28	E_D12
57	GND	GND	58	GND	GND
59	TX_D13	O_D13	60	TX_D29	E_D13
61	GND	GND	62	GND	GND
63	TX_D14	O_D14	64	TX_D30	E_D14
65	GND	GND	66	GND	GND
67	TX_D15	O_D15	68	TX_D31	E_D15
69	GND	GND	70	GND	GND
71	NC	NC	72	NC	NC
73	GND	GND	74	GND	GND
75	NC	NC	76	NC	NC
77	GND	GND	78	GND	GND
79	CLK	O_D16P/CLK	80	CLK	E_D16P/CLK
81	GND	GND	82	GND	GND
83	NC	NC	84	NC	NC
85	GND	GND	86	GND	GND
87	NC	NC	88	NC	NC
89	GND	GND	90	GND	GND
91	NC	NC	92	NC	NC
93	GND	GND	94	GND	GND
95	GND	GND	96	GND	GND
97	NC	+ 5V	98	NC	+ 5V
99	NC	+ 5V	100	NC	+ 5V

Pinning of Probe Connector J4 (Flags and Contr.) for Logic Analyser

<i>pin no.</i>	<i>signal</i>	<i>pin name (Agilent probe)</i>	<i>pin no.</i>	<i>signal</i>	<i>pin name (Agilent probe)</i>
1	GND	GND	2	GND	GND
3	NC	NC	4	NC	NC
5	GND	GND	6	GND	GND
7	FLAG_A0	O_D0	8	CONTR0	E_D0
9	GND	GND	10	GND	GND
11	FLAG_A1	O_D1	12	CONTR1	E_D1
13	GND	GND	14	GND	GND
15	FLAG_A2	O_D2	16	CONTR2	E_D2
17	GND	GND	18	GND	GND
19	FLAG_A3	O_D3	20	CONTR3	E_D3
21	GND	GND	22	GND	GND
23	FLAG_B0	O_D4	24	NC	E_D4
25	GND	GND	26	GND	GND
27	FLAG_B1	O_D5	28	NC	E_D5
29	GND	GND	30	GND	GND
31	FLAG_B2	O_D6	32	NC	E_D6
33	GND	GND	34	GND	GND
35	FLAG_B3	O_D7	36	NC	E_D7
37	GND	GND	38	GND	GND
39	FLAG_C0	O_D8	40	NC	E_D8
41	GND	GND	42	GND	GND
43	FLAG_C1	O_D9	44	NC	E_D9
45	GND	GND	46	GND	GND
47	FLAG_C2	O_D10	48	NC	E_D10
49	GND	GND	50	GND	GND
51	FLAG_C3	O_D11	52	NC	E_D11
53	GND	GND	54	GND	GND
55	FLAG_D0	O_D12	56	NC	E_D12
57	GND	GND	58	GND	GND
59	FLAG_D1	O_D13	60	NC	E_D13
61	GND	GND	62	GND	GND
63	FLAG_D2	O_D14	64	NC	E_D14
65	GND	GND	66	GND	GND
67	FLAG_D3	O_D15	68	NC	E_D15
69	GND	GND	70	GND	GND
71	NC	NC	72	NC	NC
73	GND	GND	74	GND	GND
75	NC	NC	76	NC	NC
77	GND	GND	78	GND	GND
79	CLK	O_D16P/CLK	80	CLK	E_D16P/CLK
81	GND	GND	82	GND	GND
83	NC	NC	84	NC	NC
85	GND	GND	86	GND	GND
87	NC	NC	88	NC	NC
89	GND	GND	90	GND	GND
91	NC	NC	92	NC	NC
93	GND	GND	94	GND	GND
95	GND	GND	96	GND	GND
97	NC	+ 5V	98	NC	+ 5V
99	NC	+ 5V	100	NC	+ 5V

Pinning of Probe Connector J5 (Rx_D) for Logic Analyser

<i>pin no.</i>	<i>signal</i>	<i>pin name (Agilent probe)</i>	<i>pin no.</i>	<i>signal</i>	<i>pin name (Agilent probe)</i>
1	GND	GND	2	GND	GND
3	NC	NC	4	NC	NC
5	GND	GND	6	GND	GND
7	RX_D0	O_D0	8	RX_D16	E_D0
9	GND	GND	10	GND	GND
11	RX_D1	O_D1	12	RX_D17	E_D1
13	GND	GND	14	GND	GND
15	RX_D2	O_D2	16	RX_D18	E_D2
17	GND	GND	18	GND	GND
19	RX_D3	O_D3	20	RX_D19	E_D3
21	GND	GND	22	GND	GND
23	RX_D4	O_D4	24	RX_D20	E_D4
25	GND	GND	26	GND	GND
27	RX_D5	O_D5	28	RX_D21	E_D5
29	GND	GND	30	GND	GND
31	RX_D6	O_D6	32	RX_D22	E_D6
33	GND	GND	34	GND	GND
35	RX_D7	O_D7	36	RX_D23	E_D7
37	GND	GND	38	GND	GND
39	RX_D8	O_D8	40	RX_D24	E_D8
41	GND	GND	42	GND	GND
43	RX_D9	O_D9	44	RX_D25	E_D9
45	GND	GND	46	GND	GND
47	RX_D10	O_D10	48	RX_D26	E_D10
49	GND	GND	50	GND	GND
51	RX_D11	O_D11	52	RX_D27	E_D11
53	GND	GND	54	GND	GND
55	RX_D12	O_D12	56	RX_D28	E_D12
57	GND	GND	58	GND	GND
59	RX_D13	O_D13	60	RX_D29	E_D13
61	GND	GND	62	GND	GND
63	RX_D14	O_D14	64	RX_D30	E_D14
65	GND	GND	66	GND	GND
67	RX_D15	O_D15	68	RX_D31	E_D15
69	GND	GND	70	GND	GND
71	NC	NC	72	NC	NC
73	GND	GND	74	GND	GND
75	NC	NC	76	NC	NC
77	GND	GND	78	GND	GND
79	CLK	O_D16P/CLK	80	CLK	E_D16P/CLK
81	GND	GND	82	GND	GND
83	NC	NC	84	NC	NC
85	GND	GND	86	GND	GND
87	NC	NC	88	NC	NC
89	GND	GND	90	GND	GND
91	NC	NC	92	NC	NC
93	GND	GND	94	GND	GND
95	GND	GND	96	GND	GND
97	NC	+ 5V	98	NC	+ 5V
99	NC	+ 5V	100	NC	+ 5V

Pinning of Probe Connector J6 (Testpins) for Logic Analyser

<i>pin no.</i>	<i>signal</i>	<i>pin name (Agilent probe)</i>	<i>pin no.</i>	<i>signal</i>	<i>pin name (Agilent probe)</i>
1	GND	GND	2	GND	GND
3	NC	NC	4	NC	NC
5	GND	GND	6	GND	GND
7	TEST0	O_D0	8	TEST16	E_D0
9	GND	GND	10	GND	GND
11	TEST1	O_D1	12	TEST17	E_D1
13	GND	GND	14	GND	GND
15	TEST2	O_D2	16	TEST18	E_D2
17	GND	GND	18	GND	GND
19	TEST3	O_D3	20	TEST19	E_D3
21	GND	GND	22	GND	GND
23	TEST4	O_D4	24	TEST20	E_D4
25	GND	GND	26	GND	GND
27	TEST5	O_D5	28	TEST21	E_D5
29	GND	GND	30	GND	GND
31	TEST6	O_D6	32	TEST22	E_D6
33	GND	GND	34	GND	GND
35	TEST7	O_D7	36	TEST23	E_D7
37	GND	GND	38	GND	GND
39	TEST8	O_D8	40	TEST24	E_D8
41	GND	GND	42	GND	GND
43	TEST9	O_D9	44	TEST25	E_D9
45	GND	GND	46	GND	GND
47	TEST10	O_D10	48	TEST26	E_D10
49	GND	GND	50	GND	GND
51	TEST11	O_D11	52	TEST27	E_D11
53	GND	GND	54	GND	GND
55	TEST12	O_D12	56	TEST28 *	E_D12
57	GND	GND	58	GND	GND
59	TEST13	O_D13	60	TEST29 *	E_D13
61	GND	GND	62	GND	GND
63	TEST14	O_D14	64	TEST30 *	E_D14
65	GND	GND	66	GND	GND
67	TEST15	O_D15	68	TEST31 *	E_D15
69	GND	GND	70	GND	GND
71	NC	NC	72	NC	NC
73	GND	GND	74	GND	GND
75	NC	NC	76	NC	NC
77	GND	GND	78	GND	GND
79	Test_CLK	O_D16P/CLK	80	Test_CLK	E_D16P/CLK
81	GND	GND	82	GND	GND
83	NC	NC	84	NC	NC
85	GND	GND	86	GND	GND
87	NC	NC	88	NC	NC
89	GND	GND	90	GND	GND
91	NC	NC	92	NC	NC
93	GND	GND	94	GND	GND
95	GND	GND	96	GND	GND
97, 99	NC	+ 5V	98, 100	NC	+ 5V

* only, if FLAG_D0..3 are not used !

LEDs

LED	colour	signal; high = LED on, low = LED off
1	green	TEST0
2	green	TEST1
3	green	TEST2
4	yellow	TEST3
5	yellow	TEST4
6	yellow	TEST5
7	red	TEST6
8	red	TEST7