

# Hardware Guide for High Speed PCI Card with LVDS Interface

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## History:

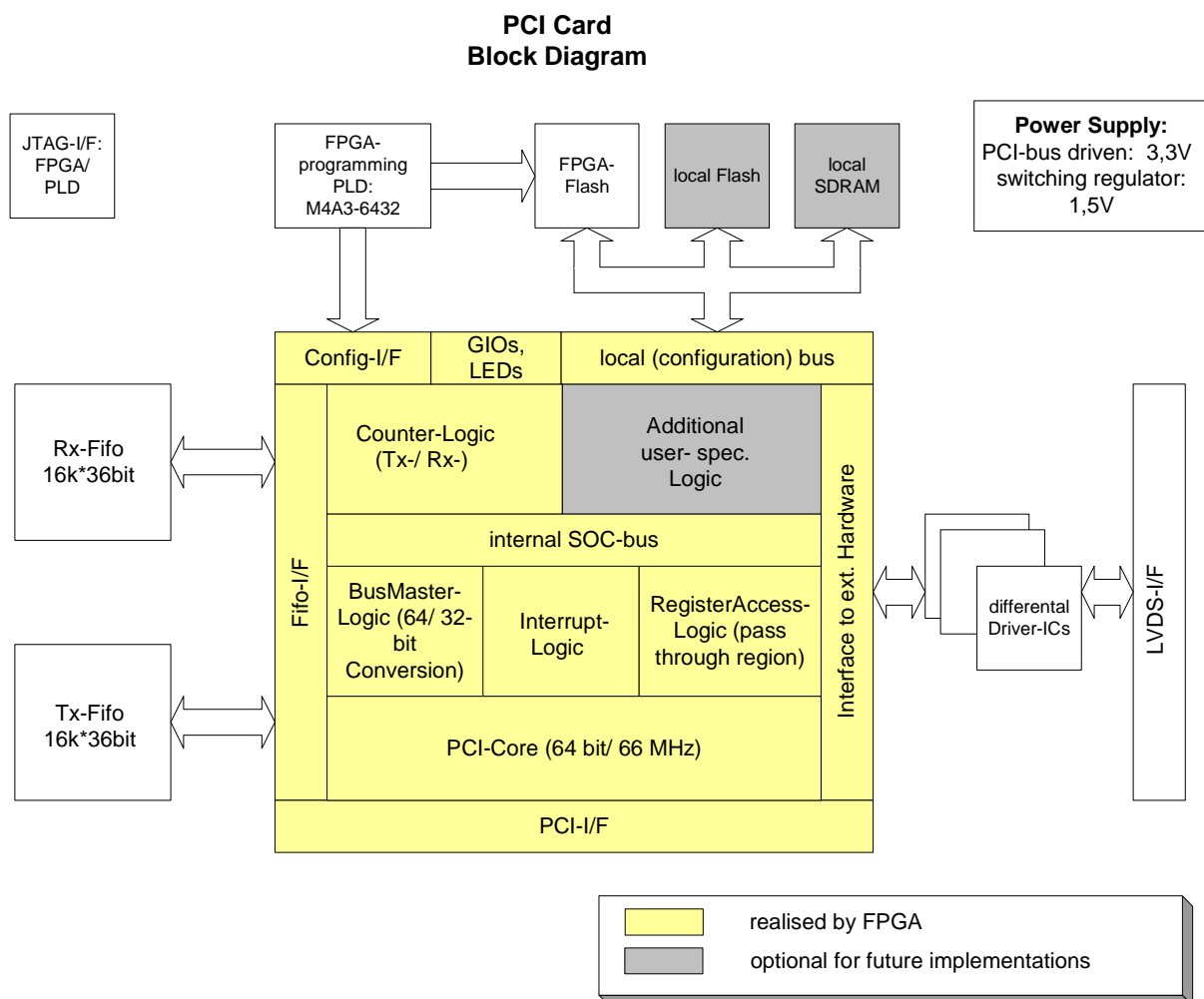
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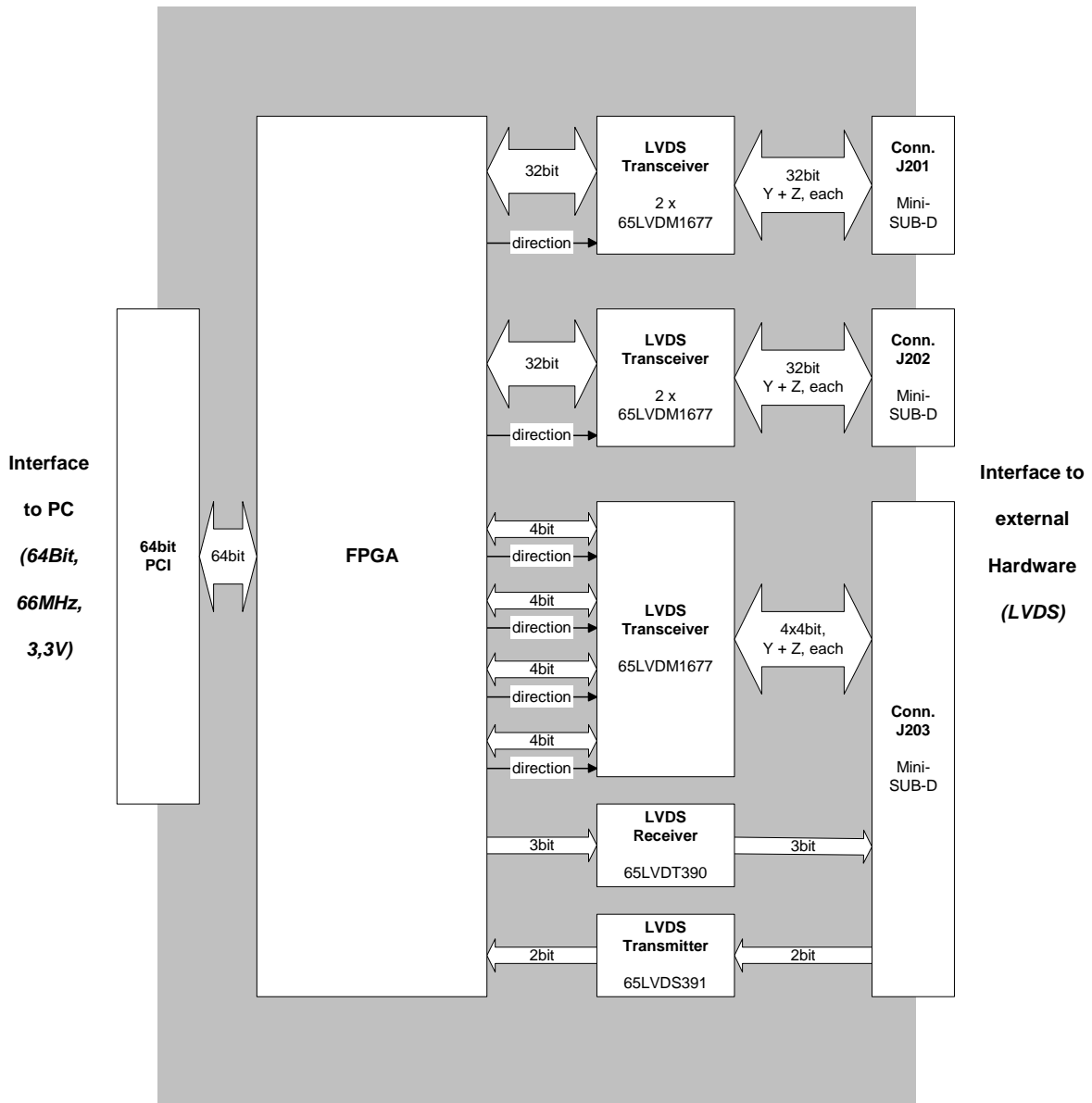
## 2. Overview on Hardware

The PCI card allows high-speed data transfer between a PC and external hardware (i. e. FPGA board, DSP). The 64bit/66MHz PCI bus is used, thus the card is predominantly suited for applications with PC server boards. The PCI card provides high on-board processing power and high flexibility, for it is equipped with an FPGA *Xilinx Virtex-II-2000*. Two 16k\*36bit FIFOs enable the PCI card to handle long data streams.



For connecting external hardware, the PCI card provides a configurable 80bit LVDS interface with additional clock and control lines. The external hardware is connected by three ribbon cables via 68pin-Mini-SUB-D connectors (female). So, for example, SCSI2-cables may be used, which are easily available as PC accessory. The integrated termination resistors are designed for a line impedance of about 100Ω.

### Overview Interfaces



### 3. Interfacing own Firmware-Modules

The PCI-card comes with a firmware, which is delivered as a PCI-core (netlist) with an example top layer and the constraint file.

The core manages the PCI transfer and provides a flexible user interface. The user interface mainly consists of:

- two 32bit data busses (*TX\_USR\_DATA*, *RX\_USR\_DATA*). At the PCI-bus, these busses are accessed via DMA. The datastreams are chained through a 64bit/32bit conversion and are buffered by the external 16k\*36 FIFOs (see *PCI Card Block Diagram*, above). The interface for the user-specific firmware is realized by small FPGA-internal FIFOs.
- the Wishbone Bus, which is accessed at PCI side via Pass Through.

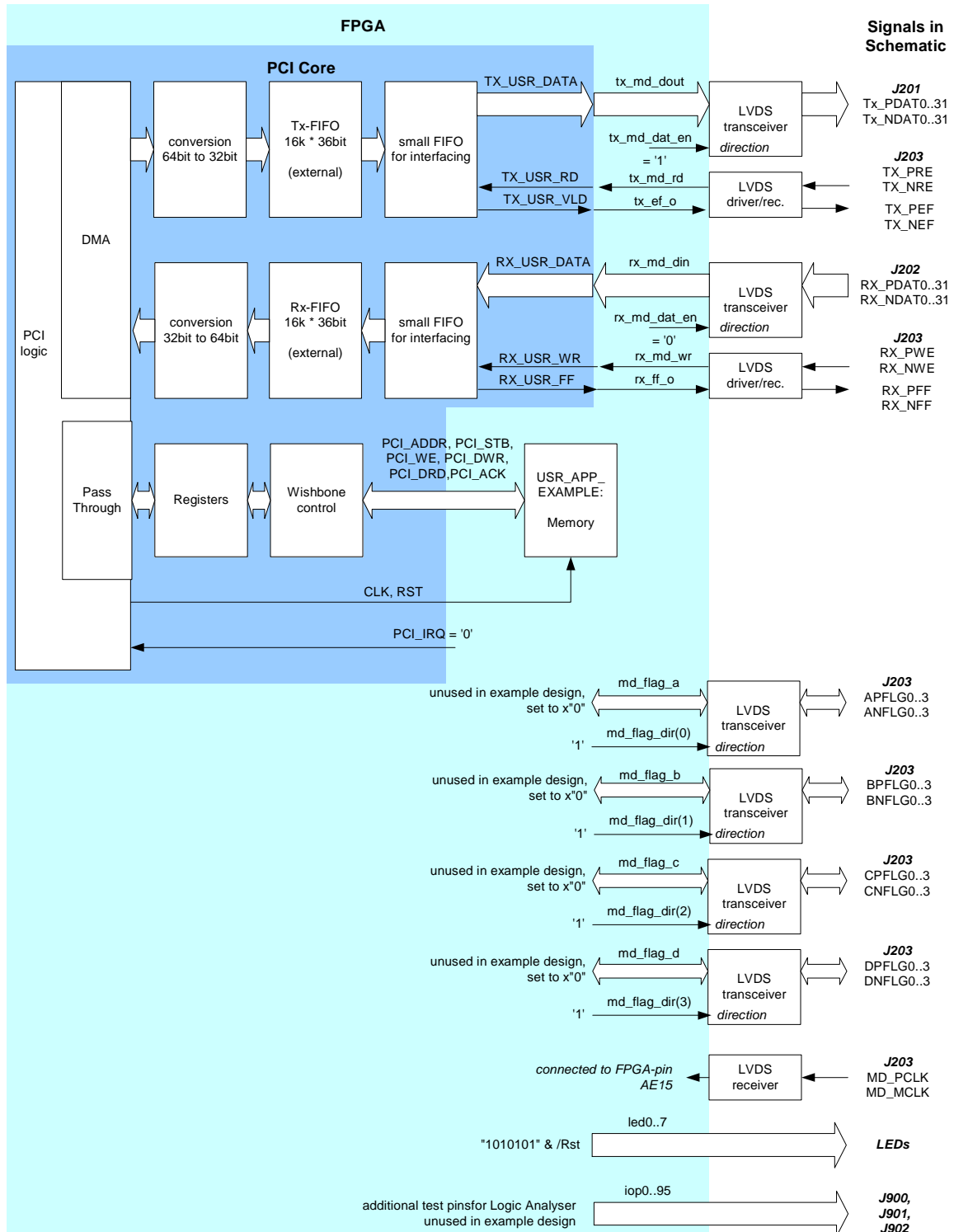
An overview on the signal flow is given in the figure below. In the delivered example top layer *TX\_USR\_DATA*, *RX\_USR\_DATA*, and the belonging control lines are directly connected to the LVDS-interface. The handling of the Wishbone Bus is demonstrated by a small example application *user\_app.vhd*, which contains a RAM instance accessible via PCI.

As you can see in the figure, there are several signals which are not used in the example design:

- The IOs *md\_flag\_a..d* can serve as additional LVDS-connections to external hardware. For example, they can be connected to the Wishbone Bus.
- The outputs *iop0..95* are connected to measurement connectors. They can flexibly be used for logic analyses. There are skew holes in the neighborhood of the connectors to allow the mounting of a small add-on boards. Please note that signal *iop52i* must stay connected to one of this IOs for routing reasons!
- There is an LVDS input *MD\_PCLK*, *MDMCLK* which can be used to supply parts of the FPGA with an external user clock. For example, *TX\_USR\_DATA*, *RX\_USR\_DATA*, ... may be referenced to the external clock by inserting asynchronous FIFOs.

Notice, that the FPGA connections to the LVDS interface (J201..203) can be monitored via test connectors J204..206. For details please refer to the schematic diagram! All test connectors fit to the ASP-adaptor which is used by the Agilent logic analysators.

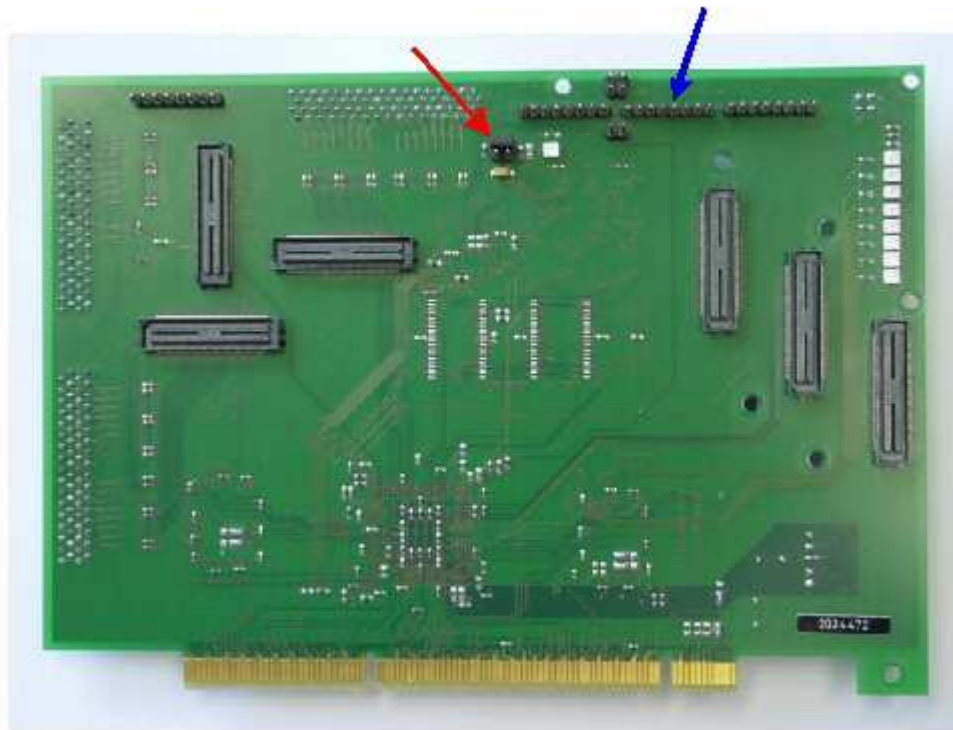
**Signal Flow**



## 4. Firmware Download

The firmware of the PCI-card is stored in a flash, which can be updated via PCI. In the flash two firmware versions are stored. So you can always keep a fallback version. The Jumper 1-2 of ST903 (red arrow in figure below) determines, which firmware will be executed:

1. Jumper is set:  
The FPGA will access the firmware stored in flash region 0 for configuration.
2. Jumper is not set:  
The FPGA will access the firmware stored in flash region 1 for configuration.



***Jumper for selecting the active firmware;  
here: the jumper is set, thus the firmware stored in region 0 will be executed.***

At the contact-pair immediately below the jumper you can connect a push-button to force an FPGA-reconfiguration after programming the flash. Note that you have to reboot your PC after reconfiguring the FPGA!

Alternatively you can switch off/on your computer to force FPGA-reconfiguration.

The handling of the configuration tool is described in the software quickguide.

If none of the configurations stored in the flash allows PCI-access, you have to program the card via JTAG. Furthermore JTAG connectivity may be required for storing test firmware only temporary or for using the ChipScope-tool provided by Xilinx. The FPGA is connected to JTAG-connector ST901, which is marked by the blue arrow in the figure above. For detailed pinning please refer to the schematic.

## 5. LVDS Interface

### 5.1 Key Data of the LVDS-Interface Devices

outgoing LVDS signals (Bus2\_D, Contr0..1, Flags):

- differential mode voltage  $|V_{OD}| = 247 \dots 454 \text{mV}$
- propagation delay 1.3 ... 3.6ns

incoming LVDS signals (Tx\_D, Contr2..3, Flags, CLK):

- differential mode voltage  $|V_{ID}| = 100 \dots 600 \text{mV}$
- common voltage  $V_{IC} = 0.5 * |V_{ID}| \dots 2.4 \text{V} - 0.5 * |V_{ID}|$
- propagation delay 1 ... 4.5ns
- termination 88 ... 132 $\Omega$

Note:

absolute maximum ratings,

specification for load 50 $\Omega$  ||10pF (Bus2\_D, Flags) resp. 100 $\Omega$  ||10pF (Contr0..1)

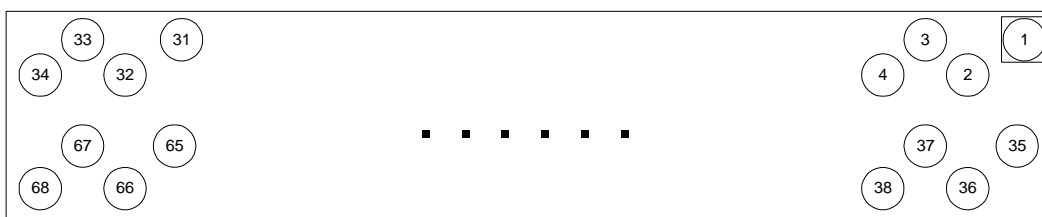
### 5.2 Connectors for the LVDS-Interface

Connector J201, J202, J203:

mini-SUB-D, 68 pin, female (cables must be fitted with male connectors),

*Harting harmik part no. 60 05 068 5100*

Pinning SUB-D; Component Side





### 5.3 Pinout of LVDS Interface

#### Connector J201: Tx Dat

<i>connector pin</i>	<i>wire no.</i>	<i>signal</i>	<i>connector pin</i>	<i>wire no.</i>	<i>signal</i>
1	1	GND	18	35	TX_PDat16
35	2	GND	52	36	TX_NDat16
2	3	TX_PDat0	19	37	TX_PDat17
36	4	TX_NDat0	53	38	TX_NDat17
3	5	TX_PDat1	20	39	TX_PDat18
37	6	TX_NDat1	54	40	TX_NDat18
4	7	TX_PDat2	21	41	TX_PDat19
38	8	TX_NDat2	55	42	TX_NDat19
5	9	TX_PDat3	22	43	TX_PDat20
39	10	TX_NDat3	56	44	TX_NDat20
6	11	TX_PDat4	23	45	TX_PDat21
40	12	TX_NDat4	57	46	TX_NDat21
7	13	TX_PDat5	24	47	TX_PDat22
41	14	TX_NDat5	58	48	TX_NDat22
8	15	TX_PDat6	25	49	TX_PDat23
42	16	TX_NDat6	59	50	TX_NDat23
9	17	TX_PDat7	26	51	TX_PDat24
43	18	TX_NDat7	60	52	TX_NDat24
10	19	TX_PDat8	27	53	TX_PDat25
44	20	TX_NDat8	61	54	TX_NDat25
11	21	TX_PDat9	28	55	TX_PDat26
45	22	TX_NDat9	62	56	TX_NDat26
12	23	TX_PDat10	29	57	TX_PDat27
46	24	TX_NDat10	63	58	TX_NDat27
13	25	TX_PDat11	30	59	TX_PDat28
47	26	TX_NDat11	64	60	TX_NDat28
14	27	TX_PDat12	31	61	TX_PDat29
48	28	TX_NDat12	65	62	TX_NDat29
15	29	TX_PDat13	32	63	TX_PDat30
49	30	TX_NDat13	66	64	TX_NDat30
16	31	TX_PDat14	33	65	TX_PDat31
50	32	TX_NDat14	67	66	TX_NDat31
17	33	TX_PDat15	34	67	GND
51	34	TX_NDat15	68	68	GND

### Connector J202: Rx Dat

<i>connector pin</i>	<i>wire no.</i>	<i>signal</i>	<i>connector pin</i>	<i>wire no.</i>	<i>signal</i>
1	1	GND	18	35	RX_PDat16
35	2	GND	52	36	RX_NDat16
2	3	RX_PDat0	19	37	RX_PDat17
36	4	RX_NDat0	53	38	RX_NDat17
3	5	RX_PDat1	20	39	RX_PDat18
37	6	RX_NDat1	54	40	RX_NDat18
4	7	RX_PDat2	21	41	RX_PDat19
38	8	RX_NDat2	55	42	RX_NDat19
5	9	RX_PDat3	22	43	RX_PDat20
39	10	RX_NDat3	56	44	RX_NDat20
6	11	RX_PDat4	23	45	RX_PDat21
40	12	RX_NDat4	57	46	RX_NDat21
7	13	RX_PDat5	24	47	RX_PDat22
41	14	RX_NDat5	58	48	RX_NDat22
8	15	RX_PDat6	25	49	RX_PDat23
42	16	RX_NDat6	59	50	RX_NDat23
9	17	RX_PDat7	26	51	RX_PDat24
43	18	RX_NDat7	60	52	RX_NDat24
10	19	RX_PDat8	27	53	RX_PDat25
44	20	RX_NDat8	61	54	RX_NDat25
11	21	RX_PDat9	28	55	RX_PDat26
45	22	RX_NDat9	62	56	RX_NDat26
12	23	RX_PDat10	29	57	RX_PDat27
46	24	RX_NDat10	63	58	RX_NDat27
13	25	RX_PDat11	30	59	RX_PDat28
47	26	RX_NDat11	64	60	RX_NDat28
14	27	RX_PDat12	31	61	RX_PDat29
48	28	RX_NDat12	65	62	RX_NDat29
15	29	RX_PDat13	32	63	RX_PDat30
49	30	RX_NDat13	66	64	RX_NDat30
16	31	RX_PDat14	33	65	RX_PDat31
50	32	RX_NDat14	67	66	RX_NDat31
17	33	RX_PDat15	34	67	GND
51	34	RX_NDat15	68	68	GND

## Connector J203: Flags and Control

<i>connector pin</i>	<i>wire no.</i>	<i>signal</i>	<i>connector pin</i>	<i>wire no.</i>	<i>signal</i>
1	1	GND	18	35	Tx_PRE
35	2	GND	52	36	Tx_NRE
2	3	APFlg0	19	37	Rx_PWE
36	4	ANFlg0	53	38	Rx_NWE
3	5	APFlg1	20	39	RX_PFF
37	6	ANFlg1	54	40	RX_NFF
4	7	APFlg2	21	41	Tx_PEF
38	8	ANFlg2	55	42	Tx_NEF
5	9	APFlg3	22	43	GND
39	10	ANFlg3	56	44	GND
6	11	BPFlg0	23	45	MD_PCLK
40	12	BNFlg0	57	46	MD_NCLK
7	13	BPFlg1	24	47	GND
41	14	BNFlg1	58	48	GND
8	15	BPFlg2	25	49	GND
42	16	BNFlg2	59	50	GND
9	17	BPFlg3	26	51	GND
43	18	BNFlg3	60	52	GND
10	19	CPFlg0	27	53	GND
44	20	CNFlg0	61	54	GND
11	21	CPFlg1	28	55	GND
45	22	CNFlg1	62	56	GND
12	23	CPFlg2	29	57	GND
46	24	CNFlg2	63	58	GND
13	25	CPFlg3	30	59	GND
47	26	CNFlg3	64	60	GND
14	27	DPFlg0	31	61	GND
48	28	DNFlg0	65	62	GND
15	29	DPFlg1	32	63	GND
49	30	DNFlg1	66	64	GND
16	31	DPFlg2	33	65	GND
50	32	DNFlg2	67	66	GND
17	33	DPFlg3	34	67	GND
51	34	DNFlg3	68	68	GND